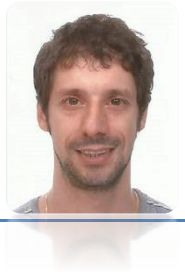
Curriculum Vitae - Paolo Burgio

PhD Electronic Engineering
BSC, MSC Computer Engineering



Personal Information

Born in: Ravenna (IT) on September 19, 1981.
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Research interests

- Autonomous Driving Systems
- Compilers and parallel programming models for many-core embedded SoCs
- Reconfigurable computing & hardware acceleration on many-core SoCs

Education and Training

BSC and MSC degrees in Computer Engineering in 2003 and 2007 respectively, at University of Bologna (IT).

- MSC thesis title*:* "Microprocessor System-on-Chip (MPSoCs) bus arbiter with Time Division Multiple Access (TDMA) predictable policy and QoS guarantee"
- My master thesis was part of a **cooperation between MicRel Lab @Università degli Studi di Bologna (IT) and ESLAB@ Linköping Universitet (SE),** where I spent 6 months. My advisors were prof. Luca Benini and prof. Petru Eles, respectively. I customized the Virtual Platform MPARM for exploring novel TDMA algorithm for the scheduling of shared bus on MPSoCs. See publication *[6]*.

PhD In Electronic Engineering in 2013, at University of Bologna (IT) and **Université de Bretagne-Sud (FR)**

- ***PhD thesis title:*** "Use of shared memory in the context of embedded multi-core processor: exploration of the technology and its limits"

Work experiences and achievements - timeline

January 2008 – June 2008

Intern researcher at ESLAB, Linköping Universitet (SE).

- I continued the work of my thesis, on TDMA algorithms for bus scheduling. My contribution was published at RTAS on 2011 (See publication *[6]*).

June 2008 – December 2009

Intern researcher @MicRel Lab (prof. Luca Benini's group), Università di Bologna, Italy.

- In 2009 my group started a cooperation with the group of prof. Buttazzo at Scuola Superiore Sant'Anna of Pisa (IT). Together, we worked on cooperative shared bus allocation and task scheduling on RT systems. The work *[1]* was published at ICCD and I presented it in Amsterdam, in 2010.

January 2010 – December 2013

PhD student at MicRel Lab (my advisor is prof. Luca Benini).

- My research activity was on exploring the applicability –and supporting- OpenMP on embedded many-core clusters. We published (*[8, 9, 10, 13]*) at **DATE 2012, 2013 and 2014**. I personally presented the works *[9, 13]* in March 2013 at Grenoble (FR) and March 2014 in Dresden (DE).
- In January 2011, I started **a joint PhD program between Università di Bologna and Université de Bretagne-Sud** (for the latter, my advisor was prof. Philippe Coussy). At UBS, I worked to extensions to the OpenMP to exploit hardware accelerators on embedded many-cores. Results of our work were accepted at DAC 2012 as a poster, and at Digital System Design – DSD 2012 as a full publication *[7]* which I presented it in Cesme (Turkey) in September 2012. Advances of this project were published at DATE 2014 *[12]*. An extended version of *[7]* was presented by me at EUC *[14]* (Milan) on August 2014.
- During 2010, I performed extensive analysis of the costs for porting the programming model OpenMP on shared memory multi-core MPSoCs, and the applicability of work stealing techniques to support workload balancing. These works were published in *[2, 3]*, and we were invited to a special issue of **MICPRO Journal** (publication *[4]*) in 2011.
- In 2011 I started a cooperation with the AI group (prof. Michela Milano) at University of Bologna. Together, we worked the optimal scheduling of tasks on Heterogeneous MPSoC Architecture. We have been accepted at Computing Frontiers –CF 2011 *[5]*.
- A report of my research in year 2012 was published in an issue of **HiPEAC Info 33** (available under request)
- I **cooperated with STMicroelectronics** for developing a SystemC wrapper to embed models of HW accelerators in a many-core multi-cluster Virtual Platform called GePop.

January 2014 - Now

Senior research staff at Università di Modena e Reggio Emilia

- My current research activity in on exploring many-core architectures for real-time systems.
- Currently I am **leading** industrial research projects for developing **autonomous driving** software
- I am developing virtual platforms for exploring many-core heterogeneous systems, and to develop/test software for them.
- I am part of the Horizon 2020 Hercules European Project, and **leading the integration work-package** for the PRYSTINE European ECSEL Project
- Teaching experience (University classes) since 2011

Cooperations

- LabSTICC, Université de Bretagne-Sud (FR), since 2010 (**Joint PhD since Jan 2011**) – *[7, 11, 12, 14]*
- ST Microelectronics (IT-FR) for VP and runtime development.
- ESLAB, Linköping Universitet (SE), in 2008-2010 (Master Thesis and advances) - *[6]*
- Embedded Systems Lab, Scuola Superiore Sant'Anna (SSSUP) of Pisa (IT), in 2009-2010 – *[1]*
- Artificial Intelligence Lab, Università di Bologna (IT) in 2010 – *[5]*

Technical skills and competences

- Programming languages for embedded systems development: C, C++, SystemC, C/OpenMP, Unix Bash
- Technologies and tools: VP (UniBo MPARM/VirtualSoC, STM GePoP), Gnu Compiler Collection (GCC-I am currently modifying it), HLS tools (Calypto CatapultC, UBS GAUT, others), GNU/Linux OS
- Programming languages for GP/web development: C#, java, ASP.NET, PHP, MySQL, MS-SQL (and tools), Visual Studio, Eclipse

Projects - timeline

- ***FP7 PREDATOR***

Year: 2009
Main activities: Virtual Platform (VP) development

- ***FP7 PRO3D***

Year: 2010
Main activities: Runtime libraries development; VP development

- ***FP7 VIRTICAL***

Year: 2011
Main Activities: Compiler development; Runtime libraries development

- ***FP7 SMECY***

Year: 2012
Main activities: Software development

- **FP7 P-*SOCRATES***

Year: 2014, 2015
Main activities: Software development and testing

- **H2020 HERCULES, POS-FESR OPEN-NEXT, ECSEL ENABLE-S3**

Year: 2016, 2017
Main activities: System design, coordination

- **H2020 HERCULES, ECSEL ENABLE-S3, ECSEL PRYSTINE, ECSEL SECREDAS, H2020 CLASS**

Year: 2018 to 2020
Main activities: System design, system integration (**WP leader**)

Awards and grants

- *August 2010:* full grant for participating to the ACACES 2010 Summer School – **Full inscription**
- *January 2011:* HiPEAC grant for participating to the CGO 2011 conference – **Full inscription & travel**
- *March 2012:* HiPEAC mobility grant for internship (UBS, Lorient, FR) – **5K Euros**
- *March 2013:* **Best poster award** at Design, Testing and Automation in Europe – DATE 2013 – **500 Euros**
- *October 2015:* **Best paper award** at CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST)

Teaching experiences

- *2016 - now*: "Parallel Programming" (Both @BSC and MSC) at Univ. of Modena
- *2014, 2015*: "Programming Basics" (C/C++) at Univ. of Modena
- *2009 to 2011*: Class in "Metodologie di Progettazione HW/SW" at Univ. of Bologna

Personal skills and competences

- *Languages:* Mothertongue italian. I have good knowledge of English, both spoken and written, which I currently use in my work. As I lived in France, I learned French. I am currently learning Spanish.

Full list of publications

2010

[1] *"Adaptive TDMA bus Allocation and Elastic Scheduling: a unified approach for enhancing robustness in multi-core RT systems",* **Paolo Burgio**, Martino Ruggiero, Francesco Esposito, Mauro Marinoni, Giorgio Buttazzo and Luca Benini*, in: 28th IEEE International Conference on Computer Design (ICCD)*, Amsterdam, Netherlands, 2010

Abstract: *We propose to integrate shared bus allocation TDMA techniques and an elastic task scheduling algorithm to deal with run-time unexpected variation of workloads in real-time systems. We prove that the overall approach significantly improves performance in real case scenarios, still ensuring the schedulabiliity of the taskset.*

[2] *"Vertical stealing: Robust, Locality-Aware Do-All Workload Distribution for 3D MPSoCs"*, Andrea Marongiu, **Paolo Burgio** and Luca Benini, in: *International Conference on Compilers Architectures and Synthesis for Embedded Systems (ESWEEK/CASES)*, Scottsdale, Arizona, 2010

Abstract:*We integrated work-stealing techniques in the OpenMP runtime support, to integrate data-locality aware static task scheduling and dynamic workload balancing on 3D multi—core systems with distributed memory and Partitioned Global Address Space (PGAS). We validated the approach with several applications.*

[3]*"Evaluating OpenMP support costs on MPSocS"*, Andrea Marongiu, **Paolo Burgio** and Luca Benini, in: *13th Euromicro Conference on Digital System Design (DSD)*, Lille, France, 2010

Abstract: *We implemented and evaluated different synchronization mechanisms, and techniques for partitioning data and meta-data to support OpenMP on multi-core shared memory clusters, performing exaustive analysis of all of the proposed algorithms. In [6] we extend this work to multiple clusters.*

2011

[4] *"Supporting OpenMP on a multi-cluster embedded MPSoC",* Andrea Marongiu, **Paolo Burgio**, Luca Benini*, **Microprocessors and Microsystems Journal**,* Volume 35, Issue 8, November 2011, Pages 668-682, ISSN 0141-9331, 10.1016/j.micpro.2011.08.010.

Abstract: *We extended the work in [11], and propose novel mechanism for synchronization and data distribution on multi-cluster many-core systems, to efficiently support OpenMP-based applications. We validated it on a Virtual Platform.*

[5] *"MPOpt-Cell: a high-performance data-flow programming environment for the CELL BE processor",* Alessio Franceschelli, **Paolo Burgio**, Giuseppe Tagliavini, Andrea Marongiu, Martino Ruggiero, Michele Lombardi, Alessio Bonfietti, Michela Milano and Luca Benini, in: *Computing Frontiers (CF) 2011*, Ischia, Italy, pages 11:1--11:2, ACM, 2011

Abstract: *We propose an integrated framework to efficiently schedule data-flow applications on the Cell B.E. architecture, maximizing the throughput of data. We prove the effectiveness of our framework on the real system.*

[6] *"Bus Access Design for Combined Worst and Average Case Execution Time Optimization of Predictable Real-Time Applications on Multiprocessor Systems-on-Chip",* Jakob Ròsen, Carl-Fredrik Neikter, Petru Eles, Zebo Peng, **Paolo Burgio** and Luca Benini*, in: Real-Time and Embedded Technology and Applications Symposium (RTAS),* 2011 17th IEEE, Chicago, IL, pages 291 - 301, 2011

Abstract*: We proposed and validated a novel off-line algorithm for shared bus scheduling on multi-core real time systems.It takes in account both Worst Case and Average Case Execution Time of the executing parallel tasks. This work is based on* ***my MSC thesis****.*

2012

[7] *"OpenMP-based Synergistic Parallelization and HW Acceleration for On-Chip Shared-Memory Clusters",* **Paolo Burgio**, Andrea Marongiu, Dominique Heller, Cyrille Chavet, Philippe Coussy and Luca Benini, in: *15th Euromicro Conference on Digital Systems Design (DSD)*, Cesme, Izmir, Turkey, pages 751 - 758, 2012.

Abstract: *We introduce a new architecture which couples application-specific Hardware Processing Units (HWPUs) to cores in tightly coupled many-core clusters. We propose extensions to OpenMP for specifying portions of code to accelerate in a C program, and developed a full toolchain for creating the platform, starting from the annotated code of a parallel+accelerated application. We validate the overall framework, enabling a mix of SW parallelization and HW acceleration in image processing applications.*

[8] *"Fast and lightweight support for nested parallelism on cluster-based embedded many-cores*", Andrea Marongiu, **Paolo Burgio** and Luca Benini, in: *Design, Automation Test in Europe Conference Exhibition (**DATE**),* 2012, pages 105-110, 2012

Abstract: *We propose –and validate- the original design of a runtime to support OpenMP-based nested parallelism on shared memory tightly-coupled many-core clusters*

2013

[9] ***"****Enabling Fine-Grained OpenMP Tasking on Tightly-Coupled Shared Memory Clusters****"***, **Paolo Burgio**, Giuseppe Tagliavini, Andrea Marongiu and Luca Benini, in: *Design, Automation Test in Europe Conference Exhibition (**DATE**),* 2013.

Abstract: *We designed an efficient runtime for supporting fine-grained OpenMP tasks on tightly coupled shared-memory many-core clusters, proposing some architectural variants for boosting up performance. We validated/characterized our design choices on a Virtual Platform, both with synthetic and real applications.*

[10] *"Variation-tolerant OpenMP Tasking on Tightly-coupled Processor Clusters",* Abbas Rahimi, **Paolo Burgio**, Andrea Marongiu and Luca Benini, in: *Design, Automation Test in Europe Conference Exhibition (**DATE**),* 2013.

Abstract: *We propose –and validate- a variation-tolerant OpenMP-based task scheduling technique for dealing with variability in many-core clustered architectures.*

[11] *"Architecture and Programming Model Support for Efficient Heterogeneous Computing on Tigthly-Coupled Shared-Memory Clusters"*, **Paolo Burgio**, Andrea Marongiu, Robin Danilo, Philippe Coussy, Luca Benini, in: *Design and Architectures for Signal and Image Processing (DASIP)*, 2013 – ***to appear***

Abstract: *We propose an architecture to overcome scalability issues in heterogeneous tightly-coupled many-core clusters, based on the so-called* Data Pump*. We also introduce low-level commodities for class-based programming paradigm of accelerators, and propose a standard API for programming them. The API has been integrated in the OpenMP frontend proposed in [4], which supports the development of modular, scalar and portable code.*

2014

[12] ***"****A tightly-coupled hardware controller to improve scalability and programmability of shared-memory heterogeneous clusters****"***, **Paolo Burgio**, Robin Danilo, Andrea Marongiu, Philippe Coussy, Luca Benini, in: *Design, Automation Test in Europe Conference Exhibition (**DATE**),* 2014.

Abstract: *We enhanced the work in [11] by proposing two optimization aimed at reducing the area of the Data Pump, improving performance at the same time. Experimental results, together with area and power estimate, prove the effectiveness of our optimizations.*

[13] *"Tightly-coupled hardware support to dynamic parallelism acceleration in embedded shared memory clusters",* **Paolo Burgio**, Giuseppe Tagliavini, Francesco Conti, Andrea Marongiu, Luca Benini, in: *Design, Automation Test in Europe Conference Exhibition (**DATE**),* 2014.

Abstract: *We propose an Hardware Scheduling Engine (HWSE) for accelerating in Hardware key primitives for supporting fine-grained tasking on embedded many-core cluster-based platforms with shared memory. We performed exhaustive analysis of the bottlenecks arising when supporting tasking on such architecture, and created a highly-optimized yet lightweight implementation in hardware for them.*

[14] *"A HLS-based toolflow to design next-generation heterogeneous many-core platforms with shared memory"*, **Paolo Burgio**, Andrea Marongiu, Philippe Coussy, Luca Benini, in: International Conference on Embedded and Ubiquitous Computing (EUC), 2014.

Abstract: *We show our fully integrated HLS-based design flow for next-generation heterogeneous embedded many-core platforms with shared memory, based on clustered design. It consists of an OpenMP frontend and compiler (with novel extensions/*pragmas *for the programming model), an HLS tool and a virtual platform for fast system prototyping.*

2015

[15] ***"****A memory-centric approach to enable timing-predictability within embedded many-core accelerators****"***, **Paolo Burgio**, Andrea Marongiu, Paolo Valente and Marko Bertogna, in *Real-Time and Embedded Systems and Technologies (RTEST)*, 2015 CSI Symposium on , vol., no., pp.1-8, 7-8 Oct. 2015. – **Best paper award**

Abstract: *In this paper, we study how the predictable execution model (PREM), a memory-aware approach to enable timing-predictability in realtime systems, can be successfully adopted on multi- and manycore heterogeneous platforms.*

[16] *"Efficient implementation of Genetic Algorithms on GP-GPU with scheduled persistent CUDA threads",* Nicola Capodieci and **Paolo Burgio**, in *Parallel Architectures, Algorithms and Programming (PAAP), 2015 Seventh International Symposium on*, vol., no., pp.6-12, 12-14 Dec. 2015

Abstract: *We present a heavily exploration oriented implementation of genetic algorithms to be executed on graphic processor units (GPUs) that is optimized with our novel mechanism for scheduling GPU-side synchronized jobs that takes inspiration from the concept of persistent threads.*

[17] *"P-SOCRATES: A parallel software framework for time-critical many-core systems",* Luís Miguel Pinho, Vincent Nélis, Patrick Meumeu Yomsi, Eduardo Quiñones, Marko Bertogna, **Paolo Burgio**, Andrea Marongiu, Claudio Scordino, Paolo Gai, Michele Ramponi and Michal Mardiak (2015), in: *Microprocessors and Microsystems*, "":"":"(-)

Abstract: *The paper presents how the time-criticality and parallelisation challenges are addressed by merging techniques coming from both HPC and EC domains, and provides an overview of the P-SOCRATES framework to achieve these objectives.*

[18] *"Simulating next-generation Cyber-physical computing platforms",* Paolo Burgio, Carlos Alvarez, Eduard Ayguadé, Antonio Filgueras, Daniel Jiménez-González, Xavier Martorell, Nacho Navarro and Roberto Giorgi, in: *De-CPS '15, Proceedings of the 2nd Workshop Challenges and New Approaches for Dependable and Cyber-Physical System Engineering.* Published in*: Ada User Journal. Dec 2015, Vol. 36 Issue 4, p259-263.*

Abstract: *In this position paper we will share our experience in the sphere of the AXIOM project, identifying key properties that virtual platforms modeling next-generation cyber-physical systems should have to quickly enable simulation-based software development for these platforms.*

2016

[19] *"A Software Stack for Next-Generation Automotive Systems on Many-Core Heterogeneous Platforms"*, **Paolo Burgio**, Marko Bertogna; Ignacio Sañudo Olmedo; Paolo Gai; Andrea Marongiu; Michal Sojka, in *2016 Euromicro Conference on Digital System Design (DSD)*, pp.55-59, 2016.

Abstract: *This paper presents the integrated software framework of the Hercules H2020 project, which allows achieving predictable performance on top of cutting-edge heterogeneous COTS platforms.*

[20] *"Enabling predictable parallelism in single-GPU systems with persistent CUDA threads"*, **Paolo Burgio**, 28th Euromicro Conference on Real-Time Systems (ECRTS16), Toulouse (FR), July 2016.

Abstract: *This paper introduces a novel software infrastructure to enable on-the-fly lightweight offload of real-time tasks onto a discrete GP-GPU accelerator. Preliminary version of code is released under GPL license and published on GitHub.*

[21] *"Embedded platforms for next-generation autonomous driving systems",* Keynote @ International Design & Test Symposium (IDT) 2016

2017

[22] *"A software stack for next-generation automotive systems on many-core heterogeneous platforms"*, **Paolo Burgio**, Marko Bertogna, Nicola Capodieci, Roberto Cavicchioli, Mickal Sojka, Houdek, Andrea Marongiu, Paolo Gai, Claudio Scordino, Bruno Morelli, in *Journal of Microprocessors and Microsystems (MICPRO), Elsevier, 2017*

Abstract: *This paper presents the software framework of Hercules H2020 project. It is an extension of paper [19]*

[23] *"Adaptive Coordination in Autonomous Driving: Motivations and Perspectives"*, Marko Bertogna; **Paolo Burgio**, Giacomo Cabri and Nicola Capodieci in *The International Conference on Enabling Technologies: Infrastructure for Collaborative Enterprises (WETICE) 2017*

Abstract: *This position paper poses some basics and challenges for when the autonomous driving technology will enter a new phase, where coordination among vehicles will be mainstream,*

[24] *" HGT: an open-source framework for simulating parallel real-time tasks"*, Ignacio Sañudo Olmedo, Paolo Burgio and Marko Bertogna, in *International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS) 2017*

Abstract: *This paper introduces the HiPeRT Generator Tool, an open-source framework that helps researchers creating synthetic yet realistic test cases, using a variety of techniques based on the model-driven development approach.*

[25] *" An emulation framework for closed source components in multi-core automotive platforms"* Ignacio Sañudo Olmedo, Paolo Burgio and Marko Bertogna, in *Forum on specification & Design Languages (FDL) 2017 - Special Session on Design and test of Automotive Embedded System*

Abstract: *This paper extends [24] adding support for Amalthea/AUTOSAR programming interface*

2018

[26] *"Convolutional Neural Networks on embedded automotive platforms: a qualitative comparison"*, **Paolo Burgio**, Gianluca Brilli, Antonio Marra, Marko Bertogna, in *Workshop on "New Platforms for Future Cars" @Design, Automation and Testing in Europa (DATE), 2018*

Abstract: *In this work, we assess the performance-per-energy of state-of-the art Convolutional Neural Network packages on next-generation embedded platforms for automotive systems*

[27] *Chapter 4 in "High-performance and time-predictable embedded computing"*, Luis Miguel Pinho, Eduardo Quinones, Marko Bertogna, Andrea Marongiu, Vincent Nelis, Paolo Gai and Juan Sancho (Editors), River Publishers, (UNDER FINAL PROOFCHECK)*, 2018*

Abstract: *In this book, we sum up the outcomes of the P-SOCRATES European project, whose goal is to pave the way to the adoption of multi-core systems as computing platforms for soft- and firm-realtime systems for embedded and high-performance computing*