Tommaso Zanotti

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Education

12/2018 - Present
PhD student – Doctoral Program in ICT
Università degli studi di Modena e Reggio Emilia - "Dipartimento di Ingegneria Enzo Ferrari", Modena (IT)

Temi di ricerca:

- *Sviluppo di architetture di calcolo innovative ad elevata efficienza energetica*
- *Elaborazione in-memory con dispositivi di memoria innovativi*
- *Modellazione compatta di dispositivi di tecnologie di memoria resistive*
- *Caratterizzazione di dispositivi di memoria*

09/2014 – 03/2017
Laurea Magistrale in Ingegneria Elettronica - 110/110 con lode
Università di Bologna "Alma Mater Studiorum" – Dipartimento di ingegneria, Bologna (IT)

Titolo Tesi: Parkinson's disease tremor monitoring using a pendant sensor in unsupervised free-living conditions.
Area di studio: Metodi numerici, progettazione di circuiti elettronici, Architetture digitali per l'elaborazione di segnali digitali, Elaborazione dei segnali.

09/2011 – 07/2014
Laurea in Ingegneria Elettronica - 110/110 con lode
Università degli studi di Modena e Reggio Emilia - Modena (IT)

Titolo tesi: Kalman Filter for Inertial Navigation Systems Applications.
Area di studio: Elettronica analogica, Misure elettroniche, Controlli automatici, Informatica.

09/2011 – 07/2014
Diploma in Elettronica e Telecomunicazioni - 100/100 con lode
I.T.I. "Enrico Fermi", Modena (IT)

Esperienza lavorativa

03/2018 – 11/2018
Test Engineer Consultant @ Ferrari S.p.a. / Maranello (Italy)

Abilità sviluppate: project management, Design of Experiments (DOE), Electronic Control Unit (ECU) Hardware and Software architectures and reliability requirements.

04/2017 – 02/2018
Co-Founder @ EasyPCR / Modena (Italy)

Abilità sviluppate: Business development, impedance- and fluorescence-based DNA sensing technologies, basic biology knowledge.

09/2016 – 03/2017
Signal Processing Intern @ Philips (Healthcare Department) / Eindhoven (Netherlands)

Abilità sviluppate: conoscenza sulle malattie neurodegenerative, algoritmi per il rilevamento di tremore, machine learning, analisi di dati relativi al cammino.

Attività di ricerca

Pubblicazioni

Conferenze e Workshops

- T. Zanotti, F. M. Puglisi and P. Pavan, " Low-Bit Precision Neural Network Architecture with High Immunity to Variability and Random Telegraph Noise based on Resistive Memories," 2021 IEEE International Reliability Physics Symposium (IRPS). (Submitted)
- T. Zanotti, F. M. Puglisi, and P. Pavan, “Circuit Reliability Analysis of In-Memory Inference in Binarized Neural Networks,” in 2020 International Integrated Reliability Workshop (IIRW), 2020 (in press). **(Best Student Paper Award)**
- T. Zanotti, F. M. Puglisi and P. Pavan, "Smart Logic-in-Memory Architecture For Ultra-Low Power Large Fan-In Operations," 2020 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), Genova, Italy, 2020, pp. 31-35, doi: 10.1109/AICAS48895.2020.9073870.
- T. Zanotti, F. M. Puglisi and P. Pavan, "Circuit Reliability Analysis of RRAM-based Logic-in-Memory Crossbar Architectures Including Line Parasitic Effects, Variability, and Random Telegraph Noise," 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2020, pp. 1-5, doi: 10.1109/IRPS45951.2020.9128343.
- T. Zanotti, F. M. Puglisi and P. Pavan, "Circuit Reliability of Low-Power RRAM-Based Logic-in-Memory Architectures," 2019 IEEE International Integrated Reliability Workshop (IIRW), South Lake Tahoe, CA, USA, 2019, pp. 1-5, doi: 10.1109/IIRW47491.2019.8989875.
- F. M. Puglisi, T. Zanotti and P. Pavan, "SIMPLY: Design of a RRAM-Based Smart Logic-in-Memory Architecture using RRAM Compact Model," ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), Cracow, Poland, 2019, pp. 130-133, doi: 10.1109/ESSDERC.2019.8901731. **(Best Paper Award)**

Riviste

- T. Zanotti, F. M. Puglisi and P. Pavan, "Multi-input Logic-in-Memory for Ultra-Low Power non-von Neumann Computing", IEEE Transactions on Emerging Topics in Computing, 2020. (Submitted)
- F. M. Puglisi, T. Zanotti and P. Pavan, "Optimized Synthesis Methodology for Ultra-Low Power Multi-Input Material Implication Logic with Emerging Non-Volatile Memories", IEEE Transactions on Emerging Topics in Computing, 2020. (Submitted)
- T. Zanotti, F. M. Puglisi and P. Pavan, "Reconfigurable Smart In-Memory Computing Platform supporting Logic and Binarized Neural Networks for Low-Power Edge Devices," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, doi: 10.1109/JETCAS.2020.3030542.
- T. Zanotti et al., "Reliability of Logic-in-Memory Circuits in Resistive Memory Arrays," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4611-4615, Nov. 2020, doi: 10.1109/TED.2020.3025271.
- T. Zanotti, F. M. Puglisi and P. Pavan, "Smart Logic-in-Memory Architecture for Low-Power Non-Von Neumann Computing," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 757-764, 2020, doi: 10.1109/JEDS.2020.2987402.
- T. Zanotti, F. M. Puglisi and P. Pavan, "Reliability-Aware Design Strategies for Stateful Logic-in-Memory Architectures," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 2, pp. 278-285, June 2020, doi: 10.1109/TDMR.2020.2981205.

Modelli compatti

- F. M. Puglisi, T. Zanotti, and P. Pavan, "Unimore Resistive Random Access Memory (RRAM) Verilog-A Model," nanoHUB, 2019, doi: 10.21981/15GF-KX29.

Eventi

- Partecipazione come oratore al IEEE International Integrated Reliability Workshop (IIRW) 2020
- Partecipazione come oratore al 2nd IEEE International Conference On Artificial Intelligence Circuits And Systems (AICAS) 2020
- Partecipazione come oratore al IEEE International Reliability Physics Symposium (IRPS) 2020
- Partecipazione alla PhD school "Electronics around the Earth" organized by the *Società Italiana di Elettronica* (SIE), Rome, 2019
- Partecipazione come oratore al SIE annual meeting, Rome, 2019
- Poster presentation at the *International Conference on Memristive Materials, Devices & Systems* (MEMRISYS), Dresden, 2019

Certificati e Riconoscimenti

- **2021 Travel Award by the Journal of Low Power Electronics and Applications (MDPI)**
- **Best student paper award at the IEEE International Integrated Reliability Workshop (IIRW) 2020.**
  T. Zanotti, F. M. Puglisi, and P. Pavan, "Circuit Reliability Analysis of In-Memory Inference in Binarized Neural Networks," in IEEE International Integrated Reliability Workshop (IIRW), 2020.
- **"Attestato di benemerenza" assegnato dal rettore dell'Università degli tudi di Modena e Reggio Emilia, Prof. C. A. Porro, il 16 Dicembre 2019.**
- **Best paper award at the IEEE European Solid-State Device Research Conference (ESSDERC) 2019.**
  F. M. Puglisi, T. Zanotti, and P. Pavan, "SIMPLY: Design of a RRAM-Based Smart Logic-in-Memory Architecture using RRAM Compact Model," in ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), 2019, pp. 130–133, doi:10.1109/ESSDERC.2019.8901731.
- **Neural Networks and Deep Learning by deeplearning.ai on Coursera 2018.**
- **Start Cup Emilia Romagna 2017 (3° place out of 134 teams)**
- **IELTS Test Score: 7.5 (2016)**
- **Texas Instruments European Analog Device Contest 2015 (Top 20 out of 300)**
  Titolo del progetto: "Power line communication in low-voltage bus smart LED lighting".