Marko Bertogna – Full Professor

Personal details

Born in Rijeka (Croatia) on October, 15th, 1977.

Nationality: Italian.

Email: marko.bertogna@unimore.it

Professional experience

From July 2020 **HiPeRT SRL** *Modena, Italy*

CEO/Founder of the academic spinoff developing autonomous systems: http://hipert.it

From November 2018 **University of Modena** *Modena, Italy*

Full Professor and leader of the High-Performance Real-Time (HiPeRT) Lab.

From November 2014 **University of Modena** *Modena, Italy*

Associate Professor and founder of the HiPeRT Lab: http://hipert.unimore.it

November 2011 – October 2014 **University of Modena** *Modena, Italy*

Tenured Assistant Professor at the Algorithmic Research Group.

September 2009 – November 2011 **Scuola Superiore S.Anna** *Pisa, Italy*

Assistant Professor at the Real-Time Systems Laboratory of the Scuola Superiore Sant'Anna, Pisa.

April 2007 – September 2009 **Scuola Superiore S.Anna** *Pisa, Italy*

Two and a half years research contract.

January 2004 – May 2008 **Scuola Superiore S.Anna** *Pisa, Italy*

PhD student with a three-year scholarship. Research in the embedded real-time systems domain at the ReTiS lab (http://retis.sssup.it/).

September 2006 – January 2007 **UNC at Chapel Hill** *North Carolina, USA*

Visiting researcher at the University of North Carolina at Chapel Hill, collaborating with prof. Sanjoy Baruah (http://www.cs.unc.edu/~baruah/).

January 2003 – January 2004 **Scuola Superiore S.Anna** *Pisa, Italy*

One-year research contract in the field of real-time systems. Analysis of Real-Time Operating Systems on FPGA platforms.

November 2001 – June 2002 **TU Delft / TU Eindhoven** *The Netherlands*

Research activity and design of integrated optical devices at the opto-electronic group of the Technische Universiteit of Delft and of Eindhoven. Scholarship of the University of Bologna.

Education

May 2008 **Scuola Superiore S.Anna** *Pisa, Italy*

Doctor of Philosophy (score *100 cum laude)* with a dissertation entitled: "Real-Time Scheduling Analysis for Multiprocessor Platforms", which received the 2010 "Giovanni Spitali" Award for the best PhD thesis at the Scuola Sant'Anna in 2008-2009.

July 2002 **University of Bologna** *Bologna, Italy*

Master in Telecommunication Engineering (score: *100 cum laude*).

1991-1996 **Liceo scientifico Belfiore** *Mantova, Italy*

Scientific high-school degree (score: *60/60*).

Research interests

Embedded real-time systems: operating systems, hypervisors, schedulers and predictable execution models for multi-/many-core platforms with GPU or FPGA acceleration.

Autonomous Driving Systems for heterogeneous operational domains: cars, racing, delivery, intra-logistics, aerial/water drones.

Honors and Awards

Fastest Autonomous Lap and **Second Place** at the first **Indy Autonomous Driving Challenge** held at Indianapolis Motor Speedway on October 23, 2021. Prize of 100.000$. Leader of the Euroracing Team.

Third Place at the second **Indy Autonomous Driving Challenge** held at Las Vegas Motor Speedway on January 7, 2023. Leader of the TII Euroracing Team, demonstrating autonomous overtaking maneuvers and speed above 270 km/h.

2010 Best Paper Award for the IEEE Transactions on Industrial Informatics (Impact Factor = 2,356) as the first author of the paper "*Resource-sharing servers for Open Environments*".

Outstanding Paper Award at the 24th International Conference on Real-Time Networks and Systems (RTNS'16), October 2016, Brest (France) for the paper *"Partitioning and Interface Synthesis in Hierarchical Multiprocessor Real-Time Systems"*.

Best Paper Award at the CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST'15), October 2015, Tehran (Iran) for the paper *"A Memory-Centric Approach to Enable Timing-Predictability within Embedded Many-Core Accelerators"*.

Outstanding Paper Award at the 27th Euromicro Conference on Real-Time Systems (ECRTS'15), June 2015, Lund (Sweden) for the paper *"Supporting Component-based Development in Partitioned Multiprocessor Real-Time Systems"*.

Best Paper Award at the 9th IEEE International Symposium on Industrial Embedded System (SIES 2014), June 2014, Pisa (Italy) for the paper *"Hard Constant Bandwidth Server: Comprehensive Formulation and Critical Scenarios"*.

Best Paper Award at the 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), August 2013, Taipei (Taiwan) for the paper *"Global Fixed Priority Scheduling with Deferred Pre-emption"*.

Best Paper Award at the 16th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2010), August 2010, Macau (China) for the paper *"Feasibility Analysis under Fixed Priority Scheduling with Fixed Preemption Points"*.

Best Paper Award at the 15th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2009), August 2009, Beijing (China) for the paper "*The Multi Supply Function Resource Abstraction for Multiprocessors: the Global EDF case*".

Best Paper Award at the 17th Euromicro Conference on Real-Time Systems (ECRTS'05), June 2005, Mallorca (Spain) as the first author of the paper *"Improved EDF multiprocessor schedulability analysis"*.

2010 "Giovanni Spitali" Award for the best PhD thesis of the Scuola Superiore Sant'Anna, Pisa, in 2008-2009.

Senior Member of the IEEE.

Board Member of the University of Mantova (Italy) since May 2017.

Stakeholder Member of the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC).

Chairing and Editorial activities

Chair of the following events:

- General Chair of Euromicro International Conference on Real-Time Systems (ECRTS'22), June 7-20, 2022, Modena, Italy.
- Program Chair of DATE Track E2 on Real-time, dependable and privacy-enhanced systems (DATE 2022).
- Program Co-Chair of DATE Track E2 on Real-time and dependable systems (DATE 2021).
- General Chair of Euromicro International Conference on Real-Time Systems (ECRTS'20), June 7-20, 2020, Modena, Italy.
- Program Co-Chair of DATE Initiative on Autonomous Systems Design (ASD 2020). March 12-13, 2020, Grenoble, France.
- Organizer of the Formula 1/10 challenge. Embedded Systems Week (ESWeek 2018). September 30-October 5, 2018. Turin, Italy.
- Organizer of the Formula 1/10 challenge. Cyber-Physical Systems Week (CPS Week 2018). April 10-13, 2018. Porto Portugal.
- Smart Mobility Track Chair of 3rd International Forum on Research and Technologies for Society and Industry, (RTSI'17), Modena, Italy, September 11-13, 2017.
- Program Chair of the 28th Euromicro International Conference on Real-Time Systems (ECRTS'17), June 27-30, 2017, Dubrovnik, Croatia.
- Program Chair of the 21st International Conference on Reliable Software Technologies (Ada-Europe 2016), June13-17, 2016, Pisa, Italy.
- Program Chair of the 6th Real-Time Scheduling Open Problems Seminar (RTSOPS'15) held in conjunction with ECRTS'15: 27th Euromicro International Conference on Real-Time Systems, July 7-10, 2015, Lund, Sweden.
- Program Chair of the 20th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA'15), Real-Time and (Networked) Embedded Systems Track, September 8-11, 2015, Luxembourg.
- Program Chair of the 5th Real-Time Scheduling Open Problems Seminar (RTSOPS'14) held in conjunction with ECRTS'14: 26th Euromicro International Conference on Real-Time Systems, July 8-11, 2014, Madrid, Spain.
- WiP Chair of the 26th Euromicro International Conference on Real-Time Systems, (ECRTS'14), July 8-11, 2014, Madrid, Spain.
- WiP Chair of the 19th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'13), April 9-11, 2013, Philadelphia, USA.
- Co-chair of the 1st Interdisciplinary Workshop on Algorithmic Challenges in Real-Time Systems (IWAC), 27-29 February 2012, Berlin, Germany.

Member of the Editorial Board of the following journals:

- Co-editor of the Real-Time Systems Journal - Special Issue on Multicore Systems, 2015 (Springer).
- Since 2015: Open Access Computer Science Journal (PeerJ).
- Since 2013: International Journal of Embedded Systems (Inderscience Publishers).
- 2013-2016: The Scientific World Journal (Hindawi Publishing Corporation).

Communications Coordinator for Europe of the Technical Committee on Real-Time Systems (TCRTS) for 2011-2015.

Chair of the Community Outreach Subcommittee of the Technical Committee on Real-Time Systems (TCRTS) from 2020.

Member of the Subcommittee on Real-Time Systems in Industrial and Factory Automation in IEEE-IES Technical Committee on Factory Automation (TCFA)

Invited Talks

Invited speaker at the following venues:

- Invited Speaker at the 2022 International Conference on Robotics and Automation (ICRA 2022) 2nd workshop on “Opportunities and Challenges with Autonomous Racing”. May 23, 2022.
- Keynote Speaker at the Euromicro Conference on Digital System Design (DSD) and Software Engineering and Advanced Applications (SEAA), Palermo, Italy. Title: “Next-Generation Embedded Platforms for Robotics”. September 2, 2021.
- Keynote Speaker at the 3rd International Conference on Intelligent Human Systems Integration: Integrating People and Intelligent Systems (IHSI 2020), Modena, Italy. Title: “A Distributed Smart Infrastructure for Autonomous Connected Vehicles”. February 19, 2020.
- Keynote Speaker at the 27th International Conference on Real-Time Networks and Systems (RTNS 2019), Toulouse, France. Title: “A View on Future Challenges for the Real-Time Community”. November 7, 2019.
- Connected City, kick-off event. Title: “The City of the Future” (100 attendees) with Suzanne Newman and Marco Gai. Turin, Italy. June 6, 2018.
- Lund University. Title: “The Future of Real-Time Systems”. LCCC Seminar series, Automatic Control Department. Lund, Sweden. May 22, 2018.
- Frontiers Conference. Title: “Are We Ready for Real Artificial Intelligence?” with Roberto Pieraccini (50 attendees). Vodafone Theater. Milan, Italy. September 21, 2017.
- TedX Modena: Failure as a Learning Experience. Title: “The Case of Autonomous Vehicles”. Modena, Stocchi Theater (600 attendees). May 27, 2017.
- Italia Digitale. Title: “The Hercules Project and the Road towards Autonomous Driving”. Milano, Gae Aulenti Auditorium (500 attendees). November 8, 2016.
- CRIT Research Seminar: the OPEN-NEXT Project. Title: “Multi-core Real-Time Systems” (80 attendees). Modena, Italy. June 30, 2016.
- Bosch Innovation. Title: “Predictable Multi-core Real-time Systems” (20 attendees). Renningen, Stuttgart, Germany. October 17, 2016.
- UPMARC 8th Summer School on Multicore Computing. Title: “Multi-core Real-Time Systems” (60 attendees). Uppsala, Sweden. June 6-9, 2016.
- ISEP/CISTER Distinguished Seminar Series. Title: “The Limited Preemption Scheduling Model” (50 attendees). Porto, Portugal, October 2nd, 2012.
- University of Luxembourg, Real-time Dependable Systems seminar series – FSTC/CSC-LASSY. Title: “EDF Scheduling for Identical Multiprocessor Systems” (50 attendees). Luxembourg. June 19th, 2012.
- INRIA/LORIA Nancy – TRIO research group. Title: “Limited Preemption Scheduling of Hard Real-Time Systems” (20 attendees). Amnéville, France. June 18th, 2012.

Committee Member

Member of the Program Committee of the following international conferences (in chronological order):

- 30th IEEE Real-Time Systems Symposium (RTSS'09), December 1-4, 2009, Washington DC, USA.
- 22nd Euromicro Conference on Real-Time Systems (ECRTS'10), July 7-9, 2010, Brussels, Belgium.
- 1st International Real-Time Scheduling Open Problems Seminar (RTSOPS'10), July 6, 2010, Brussels, Belgium.
- 16th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'10), WiP session, August 23, 2010, Macau, China.
- 31st IEEE Real-Time Systems Symposium (RTSS'10), WiP session, November 30 - December 3, 2010, San Diego, CA, USA.
- 17th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'11), WiP session, April 11-14, 2011, Chicago, IL, USA,
- 2nd International Real-Time Scheduling Open Problems Seminar (RTSOPS'11), July 5, 2011, Porto, Portugal.
- 32nd IEEE Real-Time Systems Symposium (RTSS'11), WiP session, November 29 - December 2, 2011, Vienna, Austria.
- 24th Euromicro Conference on Real-Time Systems (ECRTS'12), July 11-13, 2012, Pisa, Italy.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'12), in conjunction with 41th International Conference on Parallel Processing (ICPP'12), September 10 - 13, 2012, Pittsburgh, PA, USA.
- 17th IEEE International Conference on Emerging Technologies & Factory Automation (ETFA'12), Track 3: Real Time and Networked Embedded Systems, September 17-21, 2012, Krakow, Poland.
- 3rd International Real-Time Scheduling Open Problems Seminar (RTSOPS'12), July 10, 2012, Pisa, Italy.
- High-performance and Real-time Embedded Systems (HiRES) workshop, in conjunction with 8th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'13), January 21-23, 2013, Berlin, Germany.
- 19th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'13), Track 1: Applied Methodologies and Foundations, April 9-11, 2013, Philadelphia, USA.
- 25th Euromicro Conference on Real-Time Systems (ECRTS'13), July 9-12, 2013, Paris, France.
- 4th International Real-Time Scheduling Open Problems Seminar (RTSOPS'13), July 9, 2013, Paris, France.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'13) in conjunction with the 42nd International Conference on Parallel Processing (ICPP'13) October 1-4, 2013, Lyon, France.
- 21st International Conference on Real-Time and Network Systems (RTNS'13), 17-18 October 2013, Nice-Sophia Antipolis, France.
- 8th IEEE International Symposium on Industrial Embedded Systems (SIES '13), WiP session, June 19-21, 2013, Porto, Portugal.
- 18th IEEE International Conference on Emerging Technologies & Factory Automation (ETFA'13), Track on Real Time and Networked Embedded Systems, September 10-13, 2013, Cagliari, Italy.

- 34th IEEE Real-Time Systems Symposium (RTSS'13), WiP session, December 3-6, 2013, Vancouver, Canada.
- 2nd High-performance and Real-time Embedded Systems (HiRES'14) workshop, in conjunction with 9th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'14), January 20-22, 2014, Vienna, Austria.
- 20th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'14), WiP session, April 15-17, 2014, Berlin, Germany.
- 26th Euromicro Conference on Real-Time Systems (ECRTS'14), July 9-11, 2014, Madrid, Spain.
- 20th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'14), August 20-22, 2014, Chongqing, China.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'14) in conjunction with the 43rd International Conference on Parallel Processing (ICPP'14), September 9-12, 2014, Minneapolis, USA.
- 22nd International Conference on Real-Time and Network Systems (RTNS'14), October 8-10, 2014, Versailles, France.
- 2nd Workshop on Virtualization for Real-Time Embedded Systems (VtRES'14) in conjunction with the 19th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA'14), September 16, 2014, Barcelona, Spain.
- 19th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA'14), Track on Real Time and Networked Embedded Systems, September 16-19, 2014, Barcelona, Spain.
- 35th IEEE Real-Time Systems Symposium (RTSS'14), WiP session, December 2-5, 2014, Rome, Italy.
- 21st IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'15), April 2015, Seattle, Washington, USA.
- 27th Euromicro International Conference on Real-Time Systems (ECRTS'15), July 7-10, 2015, Lund, Sweden.
- 3rd High-performance and Real-time Embedded Systems (HiRES'15) workshop, in conjunction with 10th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'15), January 19-21, 2015, Amsterdam, Netherlands.
- 21st IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'15), August 19-23, 2015, Hong Kong.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'15) in conjunction with the 44th International Conference on Parallel Processing (ICPP'15), September 1-4, 2015, Beijing, China.
- 13th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC'15), Parallel and Distributed Systems Track, October 21-23, 2015, Porto, Portugal.
- 23rd International Conference on Real-Time and Network Systems (RTNS'15), November 4-6, 2015, Lille, France.
- 36th IEEE Real-Time Systems Symposium (RTSS'15), December 1-4, 2015, San Antonio, Texas, US
- 4th High-performance and Real-time Embedded Systems (HiRES'16) workshop, in conjunction with 11th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'16), January 18-20, 2016, Prague, Czech Republic.
- 19th Design, Automation and Test in Europe (DATE'16), Embedded Systems Software track - Real-time, Networked, and Dependable Systems, March 14-18, 2016, Dresden, Germany.

- 22nd IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'16), April 11-14, 2016, Vienna, Austria.
- 11th IEEE International Symposium on Industrial Embedded Systems (SIES '16), May 23-25, 2016, Krakow, Poland.
- 28th Euromicro International Conference on Real-Time Systems (ECRTS'16), July 5-8, 2016, Toulouse, France.
- International Workshop on Hardware/Software Interface for Internet of Things and Big Data (InterIoT&BigData'2016), in conjunction with International Conference on Parallel Processing (ICPP'2016), August 16-19, 2016, Philadelphia, PA, USA.
- 22nd IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'16), August 17-19, 2016, Daegu, Korea.
- 37th IEEE Real-Time Systems Symposium (RTSS'16), November 29-December 2, 2016, Porto, Portugal.
- 24th International Conference on Real-Time and Network Systems (RTNS'16), October 19-21, 2016, Brest, France.
- 20th Design, Automation and Test in Europe (DATE'17), Embedded Systems Software track - Real-time, Networked, and Dependable Systems, March 27-31, 2017, Lausanne, Switzerland.
- 12th IEEE International Symposium on Industrial Embedded Systems (SIES '17), June 7-9, 2017, Toulouse, France.
- 24th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'18), April 11-13, 2018, Porto, Portugal.
- 2nd CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST'18), Tehran, Iran, May 2018.
- 30th Euromicro International Conference on Real-Time Systems (ECRTS'18), July 3-6, 2018, Barcelona, Spain.
- 24th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'18), August 28-31, 2018, Hakodate, Japan.
- 26th International Conference on Real-Time and Network Systems (RTNS'18), October 10-12, 2018, Poitiers, France.
- DATE Workshop on Autonomous Systems Design (ASD 2019), March 29, 2019, Florence, Italy.
- 25th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'19), April 16-18, 2019, Montreal, Canada.
- 15th International Workshop on Factory Communication Systems (WFCS 2019), May 27-29, 2019, Sundsvall, Sweden.
- 31st Euromicro International Conference on Real-Time Systems (ECRTS'19), July 9-12, 2019, Stuttgart, Germany.
- 25th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'19), August 18-21, 2019, Hangzhou, China.
- 27th International Conference on Real-Time and Network Systems (RTNS'19), November 6-8, 2019, Toulouse, France.
- 4th Iberian Robotics Conference (ROBOT 2019), November 20-22, 2019, Porto, Portugal.
- 23rd Design, Automation and Test in Europe (DATE'20), Embedded Systems Software track - Real-time and Dependable Systems, March 9-13, 2020, Grenoble, France.
- 26th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'20), April 21-24, 2020, Sidney, Australia.
- RTNS 20, ECRTS 20, SSIV 20, RTSS 20, EMSOFT 21, ECRTS 21, RTAS 22, ECRTS 22

Reviewing Activities

Project evaluator for the following funding agencies/initiatives:

- EU Horizon 2020 ICT project Design-Operation Continuum Methods for Testing and Deployment under Unforeseen Conditions for Cyber-Physical Systems of Systems *(ADEPTNESS)*. 2020-2023.
- EU Horizon 2020 ICT project *Low Power Parallel Computing on GPUs 2 (LPGPU2)*. 2016-2018.
- Luxembourg national research fund (FNR), Research Programme CORE 2018.
- Hong Kong Research Grants Council. General Research Fund for 2018/19 and 2019/2020.
- The Swedish Knowledge Foundation – Synergi 2017 and Synergi 2018.
- ENIAC Call 2010 "TOISE" Trusted Computing for European Embedded System. 2016.
- Natural Sciences and Engineering Research Council of Canada (NSERC) - Discovery Grant (Canada) - Electrical and Computer Engineering (EG 1510). 2016.
- Italian Ministry for University and Research (MIUR) - SIR (Scientific Independence of young Researchers). 2015.

Reviewer for the following international journals:
IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Industrial Informatics, IEEE Transactions on Software Engineering, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, ACM Transactions on Embedded Computing Systems, ACM Operating Systems Review, Springer Real-Time Systems Journal, Springer Lecture Notes in Computer Science, Springer Journal of Scheduling, Springer Journal of Computer Science and Technology, Springer Journal of Signal Processing Systems, Springer International Journal on Software Tools for Technology Transfer, Elsevier Journal of Systems Architecture, Elsevier Journal of Computer and System Sciences, Elsevier Journal of Systems and Software, Elsevier Microprocessors and Microsystems, Elsevier Information Processing Letters, Hindawi Journal of Applied Mathematics, Wiley Software: Practice and Experience.

Startups

HiPeRT s.r.l. (founded in 2020) Development and Application of an Autonomous Vehicles Platform (AVP) for aerial, water/underwater and wheeled drones/robots.

Minerva Systems s.r.l. (founded in 2021) Real-Time Operating Ecosystem for High-Performance Embedded Platforms

International projects

Unit Leader of the EU project **IMOCO4**: Intelligent Motion Control under Industry 4.E (H2020-ECSEL-2020/ 101007311-2). Overall project budget: 34,586,757€ (10,163,251€ funded by the EU, 9.400.000€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 497.500€ (174.125€ funded by the EU, 135.300€ by the Italian Government). 2021-2024.

Unit Leader of the EU project **FRACTAL**: A Cognitive Fractal and Secure EDGE based on a unique Open-Safe-Reliable-Low Power Hardware Platform Node (H2020-ECSEL-2019/ 877056). Overall project budget: 16.312.778.75€ (4.933.928€ funded by the EU, 4.700.000€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 225.000€ (78.750€ funded by the EU, 63.000€ by the Italian Government). 2020-2023.

Unit Leader of the EU project **InSecTT** - Intelligent Secure Trustable Things (H2020-ECSEL-2019/ 877056). Overall project budget: 48.858.334€ (11.489.516€ funded by the EU, 14.135.379€ by national authorities). Budget assigned to the Research Unit of the Italian Inter-University Consortium for Informatics (CINI): 2.338.125€ (818.343€ funded by the EU, 605.812€ by the Italian Government). Budget for HiPeRT Lab: 200.000€ (70.000€ by EU, 60.000€ by Italian Gov.). 2020-2023.

Unit Leader of the EU project **NEWCONTROL**: Integrated, Fail-Operational, Cognitive Perception, Planning and Control Systems for Highly Automated Vehicles (H2020-ECSEL-2018/826653). Overall project budget: 48.629.823€ (14.036.162€ funded by the EU, 13.932.519€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 425.000€ (148.750€ funded by the EU, 127.500€ by the Italian Government). 2019-2022.

Vice Coordinator and **Unit Leader** of the EU project **CLASS**: Edge and CLoud Computation: A Highly Distributed Software Architecture for Big Data AnalyticS (H2020-ICT-2017-1/ 780622). Overall project budget: 3.900.803€ (entirely funded by the EU). Budget assigned to the Research Unit of the University of Modena: 492.166€ (entirely funded by the EU). 2018-2021.

Unit Leader of the EU project **PRYSTINE**: Programmable Systems for Intelligence in Automobiles (H2020-ECSEL-2017/783190). Overall project budget: 51.000.000€ (14.500.000€ funded by the EU, 14.500.000€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 525.000€ (183.750€ funded by the EU, 157.500€ by the Italian Government). 2018-2021.

Unit Leader of the EU project **SECREDAS**: Cyber Security for Cross Domain Reliable Dependable Automated Systems (H2020-ECSEL-2016/783119). Overall project budget: 51.500.000€ (14.900.000€ funded by the EU, 16.000.000€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 500.000€ (175.000€ funded by the EU). 2018-2021.

Participant to the EU project **5G-CARMEN**: 5G for Connected and Automated Road Mobility in the European UnioN (H2020-ICT-2018/ 210493808). Overall project budget: 15.000.000€ (entirely funded by the EU). Budget assigned to the Research Unit of CNIT: 594.375€ (entirely funded by the EU). Budget for HiPeRT Lab: 65.000€ (entirely funded by EU). 2018-2021.

Unit Leader of the EU project **I-MECH**: Intelligent Motion Control Platform for Smart Mechatronic Systems (H2020-ECSEL-2016/737453). Overall project budget: 17.003.102€ (5.018.645€ funded by the EU, 4.900.000€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 488.750€ (171.062€ funded by the EU, 146.625€ by the Italian Government). 2017-2020.

Coordinator of the EU project **HERCULES**: High-Performance Real-time Architectures for Low-Power Embedded Systems (H2020/ICT/2015/688860). Overall project budget: 3.261.299€ (2.780.923€ funded by EU and Switzerland). Budget assigned to the Research Unit of the University of Modena: 606.549€ (entirely funded by the EU). 2016-2019.

Unit Leader of the EU project **ENABLE-S3**: European Initiative to Enable Validation for Highly Automated Safe and Secure Systems (H2020-ECSEL-2015/692455). Overall project budget: 68.135.913€ (16.651.856€ funded by the EU, 16.651.856€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 216.563€ (86.625€ funded by the EU, 54.140€ by the Italian Government). 2016-2019.

Vice Coordinator and **Unit Leader** of the EU project **P-SOCRATES**: Parallel Software Framework for Time-Critical Many-Core Systems (FP7/2013/ICT/611016). Overall project budget: 3.624.942€ (2.762.000€ funded by the EU). Budget assigned to the Research Unit of the University of Modena: 492.200€ (378.400€ funded by the EU). 2013-2017.

Unit Leader of a Technology Transfer Project (TTP) within EU project **TETRACOM** (FP7-ICT-2013/609491). TTP: SemBoost: order-of-magnitude performance Boost for a leading Semantic engine. Budget assigned to the Research Unit of the University of Modena: 70.000€ (30.000€ funded by the EU). 2015-2016.

Management Committee (MC) Member for Italy of the EU project **TACLe**: Timing Analysis on Code-Level (ICT COST Action IC1202). Overall budget: 120.000€ (entirely funded by the EU). 2012-2016.

Participant to the EU project **ACTORS**: Adaptivity and Control of Resources in Embedded Systems (FP7/2008/ICT/216586). 2008-2012.

Unit Leader of the EU project **PREDATOR**: Design for Predictability and Efficiency (FP7/2008/ICT/216008). Budget assigned to the Research Unit of Scuola Sant'Anna: 398.200€ (299.400€ funded by the EU). 2008-2011.

Participant to the EU project **IRMOS**: Interactive Realtime Multimedia Applications on Service Oriented Infrastructures (FP7/2007/ICT/214777). 2008-2011.

Participant to the EU project **FRESCOR**: Framework for Real-time Embedded Systems based on Contracts (FP6/2005/IST/5-034026). 2006-2009.

National and Industrial projects

Unit Leader of the POR-FESR 2014-2020 project CEMP: Connected Electric modular Powertrain. Overall project budget: 6.444.282€ (2.730.183€ funded by the EU through the Lombardia region). Budget assigned to the Research Unit of the University of Modena: 935.056€ (374.022€ funded by the EU through the Lombardia region). 2/12/2019 – 31/05/2022.

Unit Leader of project "Mantova: a Distributed Territorial Laboratory for Innovation and Employability – funded by Cariverona Foundation under the Grant "Azioni di Sistema per la Valorizzazione dei Territori". Overall project budget: 715.000€ (500.000€ funded by Cariverona Foundation). Budget assigned to the Research Unit of the University of Modena: 75.000€ (60.000€ funded by Cariverona). 1/1/2019 – 31/12/2021.

Unit Leader of Design of POR-FSE 2014-2020 project: A New-Generation Black-Box with Advanced Functionalities for Semi-Autonomous, Sensorized and Connected Vehicles. Grant for High-Competence New Startups within the Emilia Romagna Regional Lab for Entrepreneurship. Budget assigned to the Research Unit of the University of Modena: 60.000€ (52.000€ funded by the EU through the Emilia Romagna region). 2020-2021.

Unit Leader of the POR-FESR 2014-2020 project OPEN-NEXT: Open-source Software Templates for Next-Generation Industrial Embedded Platforms. Overall project budget: 1.021.250€ (739.250€ funded by the EU through the Emilia Romagna region). Budget assigned to the Research Unit of the University of Modena: 305.000€ (219.500€ funded by the EU through the Emilia Romagna region). 01/04/2016 – 31/03/2018

Expert System s.p.a.: Parallelization and Performance Improvement of a C-based Semantic Engine. Overall budget: 36.600€ (entirely funded by the company). 18/07/2014 – 31/12/2014

Doxee s.r.l.: Performance Analysis of a Java-based Document Management Engine. Overall budget: 18.300€ (entirely funded by the company). 1/12/2014 – 31/05/2015

Doxee s.r.l.: Performance Optimization and Memory Occupancy Minimization of a Java-based Application for the Massive Production of Data-variable Documents on Multi-core Servers. Overall budget: 12.200€ (entirely funded by the company). 1/04/2016 – 31/07/2016

Egicon s.r.l.: Profiling of Real-Time Systems Executing upon an Embedded Multi-core Platform. Overall budget: 36.600€ (entirely funded by the company). 2/08/2016 – 31/08/2017

Doxee s.r.l.: Design and Implementation of a New Distributed On-demand Production System and Setup of a Competence Center on Document Composition. Overall budget: 91.500€ (entirely funded by the company). 01/09/2016 – 28/02/2018.

Nvidia Corporation: GPU Real-Time Computing and Scheduling. Overall budget: 114.198$ (entirely funded by the company). 20/03/2017 – 19/09/2017.

SACMI Imola S.C.: Heterogeneous Multi-core Platforms for Real-Time Applications. Overall budget: 48.800€ (entirely funded by the company). 01/02/2017 – 31/01/2018.

Bosch GmbH: funding of a 3-years PhD scholarship on Real-Time Multi-core Systems for Automotive Applications. 1/10/2017 – 30/09/2020.

TETRA PAK Packaging Solutions S.p.A.: Real-time analysis and assessment of multi-core platforms for industrial motion and control. Overall budget: 25.000€ + VAT (entirely funded by the company). 17/10/2017 – 16/04/2018.

NEOS s.r.l.: Analysis and implementation of parallel algorithms for dithering/half toning in the digital printing domain. Overall budget: 36.600€ (entirely funded by the company). 01/02/2017 – 31/01/2018.

Participant to the FAR 2017 project funded by UNIMORE on "the Future of Autonomous Driving Vehicles: technological solutions and ethics/legal problems for resilient solutions to human errors and cyber-attacks. Overall budget: 80.000€ (entirely funded by UNIMORE). 01/02/2018-31/1/2020.

Xilinx Inc.: Implementation of a hypervisor-based cache coloring mechanism for industrial real-time applications. Overall budget: 25.292€ + VAT (entirely funded by the company). 08/01/2018 – 30/06/2018.

Nvidia Corporation: Real-time scheduling of GPU resources and recommendations for architectural enhancements. Overall budget: 128.290$ (entirely funded by the company). 05/02/2018 – 04/08/2018.

Generali: study of insurance policies for autonomous driving. 1/2/2018 – 31/1/2019.

Maserati S.p.A.: Machine learning algorithms for the automotive domain. Overall budget: 45.750€ + VAT (entirely funded by the company). 01/04/2018 – 31/12/2018.

Bosch GmbH: Code Generation Tool for Heterogeneous Hardware Platforms based on Amalthea. Overall budget: 40.000€ + VAT (entirely funded by the company). 1/7/2018 – 31/03/2019.

United Technologies Research Center (UTRC): Predictable hypervisor and multi-OS support for heterogeneous hardware platforms. Overall budget: 12.500$ + VAT (entirely funded by the company). 11/9/2018 – 31/12/2018.

TETRA PAK Packaging Solutions S.p.A.: Real-time analysis and assessment of multi-core platforms for industrial motion and control (extension). Overall budget: 30.000€ + VAT (entirely funded by the company). 16/04/2018 – 31/3/2019.

Ferrari S.p.A.: co-funding of a research fellowship on next-generation ADAS applications. Overall budget: 28.000€ (9.000 funded by Ferrari, 19.000€ by the Emilia Romagna region through POR-FSE 2014-2020 project Automotive Academy. 1/2/2019 – 31/1/2020.

Xilinx Inc.: Implementation of cache coloring mechanism in the Xen hypervisor. Overall budget: 30.000€ + VAT (entirely funded by the company). 01/02/2019 – 31/07/2019.

Ferrari S.p.A.: Study and Prototyping of ADAS 2.0 systems on High-Performance Embedded Platforms. Overall budget: 95.000€ (entirely funded by the company). 1/3/2019 – 28/2/2020.

TETRA PAK Packaging Solutions S.p.A.: Machine-Learning Algorithms for Data-driven Forming Quality Prediction. Overall budget: 60.000€ + VAT (entirely funded by the company). 01/04/2020 – 31/3/2021.

Maserati S.p.A.: Machine-Learning Algorithms for Driver's Drowsiness Level Identification. Overall budget: 70.000€ + VAT (entirely funded by the company). 01/12/2019 – 31/12/2020.

Maserati S.p.A.: Characterization of high-Performance Embedded Computing Platforms for the Automotive Domain. Budget: 80.000€ + VAT (entirely funded by the company). 01/11/2019 – 30/05/2020.

Huawei Technologies Co., Ltd.: Real-Time Computing with AI Accelerators. Overall budget: 70.000$ + VAT (entirely funded by the company). 01/02/2020 – 31/01/2021.

System Logistics S.p.A.: New Hardware/Software Architecture for Autonomous Vehicles. Overall budget: 70.000€ + VAT (entirely funded by the company). 01/02/2020 – 31/12/2020.

ARM Ltd.: CMN-600 Characterization for real-time workloads. Overall budget: 50.000€ + VAT (entirely funded by the company). 01/04/2020 – 30/10/2020.

Coordinator and **Unit Leader** of the UAE project "Development of a State-of-the-Art Autonomous Vehicles Platform" funded by the Technology Innovation Institute (TII). Overall project budget: 3.281.000€ (entirely funded by TII). Budget assigned to the Research Unit of the University of Modena: 1.210.000€ (entirely funded by TII). 2020-2023. The project aims at developing a swarm of autonomously aerial drones of micro and nano-size, able to explore and map unknown environments with no human intervention.

Coordinator and **Unit Leader** of the UAE project "Ground, Surface and Underwater Autonomous Vehicles " funded by the Technology Innovation Institute (TII). Overall project budget: 3.320.000€ (entirely funded by TII). Budget assigned to the HiPeRT Srl: 2.100.000€ (entirely funded by TII). 2020-2023. The project aims at developing an Unmanned Ground Vehicle (UGV), an Autonomous Surface Vehicles (ASV), and an Underground Autonomous Vehicle (UAV) to explore and map unknown environments with no human intervention.

Coordinator of the Euroracing team participating to the first Indy Autonomous Challenge 350.000€ (entirely funded by TII).

Coordinator of the UAE project "Autonomous Racing Cars" funded by the Technology Innovation Institute (TII). Overall project budget: 1.200.000€ (entirely funded by TII). 2021-2024.

Coordinator of the UAE project " LR-UAV: Long-Range Underwater Autonomous Vehicle" funded by the Technology Innovation Institute (TII). Overall project budget: 350.000€ (entirely funded by TII). 2021-2024.

Coordinator of Regional project OpenAir - Automatic detection system of the social distancing requirement in open spaces to support the Municipal Police, POR-FESR Emilia-Romagna. Overall project budget assigned to the University of Modena: 150.000€ (120.000€ funded by the EU through the Emilia Romagna region). 2020-2021.

Vice Coordinator of Regional project IoMiMuovo: Sistema di rilevazione automatica del requisito di distanziamento sociale per trasporto pubblico urbano ed extraurbano, POR-FESR Emilia-Romagna. Overall project budget assigned to the University of Modena: 150.000€ (120.000€ funded by the EU through the Emilia Romagna region). 2020-2021.

Lifetouch Srl: Optimization of image detection software. Overall project budget: 30.000€ (entirely funded by the company). 2020-2021.

Lynx Software Technologies Inc.: Analysis of Lynx's MOSA.ic platform. Overall budget: 25.000$ + VAT (entirely funded by the company). 21/07/2020 – 20/01/2021.

Unit Leader of UAE project "RISC-V-Based Secure Drone Platform" funded by the Technology Innovation Institute (TII). Overall project budget: 2.110.000€ (entirely funded by TII). Budget assigned to the Research Unit of the University of Modena: 870.000€ (entirely funded by TII). 2021-2024.

Unit Leader of UAE project "Next generation RISC-V-Based Secure Flight Computer System" funded by the Technology Innovation Institute (TII). Overall project budget: 1.600.000€ (entirely funded by TII). Budget assigned to HiPeRT Srl: 883.700€ (entirely funded by TII). 2021-2024.

IVECO DV Spa: Consultancy on the design and scouting of autonomous driving systems. Overall budget: 25.000€ + VAT (entirely funded by the company). 14/01/2022 – 13/05/2020.

Nvidia Corporation: Analysis of AV System Scheduler (STM) for autonomous driving". Overall budget: 80.400€ (entirely funded by the company). 24/06/2021 – 23/01/2022.

CNH Industrial Italia Spa: Characterization of High Performance Embedded Computing Platforms. Overall budget: 25.000€ + VAT (entirely funded by the company). 01/10/2021 – 31/03/2022.

OCME: Localization and natural navigation of autonomous vehicles in an unstructured environment. Overall budget: 100.000€ + VAT (entirely funded by the company). 04/06/2020 – 31/12/2022

System Logistics: New hardware and software architecture for autonomous vehicles. Overall budget: 70.000€ + VAT (entirely funded by the company). 27/02/2020 – 31/05/2021

Unit Leader of the PRIN 2017 project SPHERE: Software architecture for Predictable HEterogeneous REal-time systems (Prot. 20172NNB4T). Overall project budget: 697.300€ (547.300€ funded by MIUR). Budget assigned to the Research Unit of the University of Modena: 169.000€ (137.000€ funded by MIUR). 01/09/2019 – 30/08/2022.

Abaco Spa: Design of Algorithms for Data Analysis and Decision Support Systems. Overall budget: 30.000€ + VAT (entirely funded by the company). 25/03/2020 – 24/03/2022

Huawei Technologies Sweden AB: Schedulability Study of Conditional DAG for Parallel Exection of 5G Baseband SW on Multi-Core SoC Systems. Overall budget: 110.000€ + VAT (entirely funded by the company). 01/11/2020 – 31/10/2021.

Ferrari S.p.A.: Improvement of a new generation ADAS system. Overall budget: 10.000€ (entirely funded by the company). 1/11/2021 – 31/12/2021.

Xilinx Inc.: High-performance PL-based inter-domain communication. Overall budget: 40.000€ + VAT (entirely funded by the company). 26/01/2022 – 25/07/2022.

Unit Leader of EIT Urban Mobility 2022-2024 project IPA2X: Intelligent Pedestrian Assistant to Everyone. Overall project budget: 1.300.000€ (911.000€ funded by European Institute of Innovation and Technology). Budget assigned to the Research Unit of HiPeRT Srl: 132.870€ (93.010€ funded by EIT). 2022.

Teaching activity	Responsible of the course "**Platforms and Algorithms for Autonomous Driving**" course (72 hours, 9 credits) for the Master Degree in Advanced automotive electronic engineering of the University of Modena, Italy, from 2019 on.
	Responsible of the course "**Real-Time Embedded Systems**" (72 hours, 9 credits) for the Master Degree in Computer Engineering of the University of Modena, Italy, from 2017 on.
	Responsible of the course "**Computer Architectures**" (72 hours, 9 credits) for the Degree in Computer Science of the University of Modena, Italy, from 2017 on.
	Responsible of the "**High-Performance Computing**" course (48 hours, 6 credits) for the Master Degree in Computer Science of the University of Modena, Italy, for the academic year 2018-2019.
	Responsible of the "**Advanced Programming**" course (72 hours, 9 credits) for the Degree in Computer Science of the University of Modena, Italy, for the academic year 2011-2012, 2012-2013, 2013-2014, 2014-2015, 2015-2016 and 2016-2017.
	Responsible of the "**Advanced Parallel Programming**" course (48 hours, 6 credits) for the Master Degree in Computer Science of the University of Modena, Italy, for the academic years 2016-2017, 2017-2018.
	Course on "**Embedded Systems for Automotive**" (20 hours) for Alfa/Maserati's PD Training Program, batches January 2017, July 2017.
	Responsible of three different courses on "**Computer Science**" (24 hours, 3 credits) for various degrees in 2015-2016 (3 classes), 2016-2017.
	Teaching Assistant of the "**Basic Computer Science**" course (20 hours, 2 credits) for different degrees of the University of Modena, Italy, for the academic years 2012-2013 and 2013-2014, 2014-2015.
	Responsible of the "**Computer Architectures**" course (94 hours, 9 credits) for the Degree in Automation Engineering of the University of Siena, Italy, for the academic year 2010-2011.
	Responsible of the "**Real-Time Operating Systems**" course (52 hours, 5 credits) for the Degree in Automation Engineering of the University of Siena, Italy, for the academic years 2008-2009, 2009-2010 and 2010-2011.
	Responsible of the "**Multiprocessor Scheduling**" course (2x10 hours, 2x1 credits) for PhD and Master students on Computer Science of the Scuola Sant'Anna, Pisa, Italy, for the academic year 2009-2010.
	Responsible of the "**Multicore Systems**" course at the ERICSSON Research Center of Rome, Italy (16 hours), July 2008.
Personal life	Married with Lidia Maria Diaz Monzon (since September 2008).
	Proud father of three children: Luca (April 22, 2010), Diego (April 20, 2013) and Sofia (August 7, 2020).
Languages	Italian, English and Spanish: excellent level.
	Croatian, German and French: good level.

Modena, January 10th, 2022
Marko Bertogna

Major publications

Marko Bertogna is author of over 100 papers in international journals and peer-reviewed conferences, mainly in the field of real-time and embedded systems. His main interests are in the analysis and design of scheduling algorithms for single, multi- and many-core systems, protocols for the access to shared resources, resource-reservation techniques. His works collected more than 4000 citations, with an h-index of 38 (source: Google Scholar). A list of the major publications follows.

Books

1) Sanjoy Baruah, Marko Bertogna, Giorgio Buttazzo, "*Multiprocessor Scheduling for Real-Time Systems*", Springer International Publishing, Embedded Systems Series, 2015.
2) Luis Miguel Pinho, Eduardo Quinones, Marko Bertogna, Andrea Marongiu, Vincent Nélis, Paolo Gai, Juan Sancho,,"*High-Performance and Time-Predictable Embedded Computing*", River Publishers, Series in Information Science and Technology, 2018.

International Journals

3) Falk Rehm, Dakshina Dasari, Arne Hamann, Michael Pressler, Dirk Ziegenbein, Joerg Seitter, Ignacio Sañudo, Nicola Capodieci, Paolo Burgio, Marko Bertogna, "*Performance modeling of heterogeneous HW platforms*", Microprocessors and Microsystems, 87. November 2021.
4) Björn Forsberg, Marco Solieri, Marko Bertogna, Luca Benini, Andrea Marongiu, "*The predictable execution model in practice: Compiling real applications for COTS hardware*", ACM Transactions on Embedded Computing Systems (TECS), 20(5), 1-25. July 2021.
5) Alessandro Biondi, Daniel Casini, Giorgiomaria Cicero, Niccolò Borgioli, Giorgio Buttazzo, Gaetano Patti, Luca Leonardi, Lucia Lo Bello, Marco Solieri, Paolo Burgio, Ignacio Sanudo Olmedo, Angelo Ruocco, Luca Palazzi, Marko Bertogna, Alessandro Cilardo, Nicola Mazzocca, Antonino Mazzeo, "*SPHERE: A Multi-SoC Architecture for Next-Generation Cyber-Physical Systems Based on Heterogeneous Platforms*", IEEE Access, 9. May 2021.
6) Jorge Martinez, Dakshina Dasari, Arne Hamann, Ignacio Sañudo, Marko Bertogna, "*Exact response time analysis of fixed priority systems based on sporadic servers*", Journal of Systems Architecture, 10. November 2020.
7) Houssam-Eddine Zahaf, Nicola Capodieci, Roberto Cavicchioli, Giuseppe Lipari, Marko Bertogna, "*The HPC-DAG task model for heterogeneous real-time systems*", IEEE Transactions on Computers, 70(10). September 2020.
8) Nicola Capodieci, Paolo Burgio, Roberto Cavicchioli, Ignacio Sanudo Olmedo, Marco Solieri, Marko Bertogna, "*Real-time requirements for ADAS platforms featuring shared memory hierarchies*", IEEE Design & Test. August 2020.
9) Jorge Martinez, Ignacio Sanudo, Marko Bertogna, "*End-To-End Latency Characterization of Task Communication Models for Automotive Systems*", Real-Time Systems: The International Journal of Time-Critical Computing. 56 (3), 315-347. Springer. June 2020.
10) Houssam-Eddine Zahaf, Giuseppe Lipari, Marko Bertogna, Pierre Boulet, "*The Parallel Multi-Mode Digraph Task Model for Energy-Aware Real-Time Heterogeneous Multi-Core Systems*", IEEE Transactions on Computers. 68 (10), 1511-1524. October 2019.
11) Jorge Martinez, Ignacio Sanudo, Marko Bertogna, "*Analytical Characterization of End-to-End Communication Delays with Logical Execution Time*". IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). 37(11). November 2018.
12) Alessandro Biondi, Giorgio Buttazzo, Marko Bertogna, "*A design flow for supporting component-based software development in multiprocessor real-time systems*". Real-Time Systems: The International Journal of Time-Critical Computing. 54 (4), 800-829. Springer. March 2018.
13) Paolo Burgio, Marko Bertogna, Nicola Capodieci, Roberto Cavicchioli, Michal Sojka, Přemysl Houdek, Andrea Marongiu, Paolo Gai, Claudio Scordino, Bruno Morelli, "*A software stack for next-*

generation automotive systems on many-core heterogeneous platforms". Microprocessors and Microsystems. Volume 52, 299-311. Elsevier. July 2017.

14) Alessandra Melani, Marko Bertogna, Robert I. Davis, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio C. Buttazzo. *"Exact Response Time Analysis for Fixed Priority Memory-Processor Co-scheduling"*, IEEE Transactions on Computers. 66 (4), 631-646. April 2017.
15) Alessandra Melani, Marko Bertogna, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio C. Buttazzo. *"Schedulability Analysis of Conditional Parallel Task Graphs in Multicore Systems"*, IEEE Transactions on Computers. 66 (2), 339-353. February 2017.
16) Alessandro Biondi, Giorgio Buttazzo, Marko Bertogna, *"Schedulability Analysis of Hierarchical Real-Time Systems under Shared Resources"*, IEEE Transactions on Computers. 65(5): 1593-1605. May 2016.
17) Robert I. Davis, Liliana Cucu-Grosjean, Marko Bertogna, Alan Burns, *"A Review of Priority Assignment in Real-Time Systems"*, Elsevier Journal of Systems Architecture. 65(C): 64-82, April 2016.
18) Robert I. Davis, Marko Bertogna, Vincenzo Bonifaci, "*On the Compatibility of Exact Schedulability Tests for Global Fixed Priority Pre-emptive Scheduling with Audsley's Optimal Priority Assignment Algorithm*", Real-Time Systems: The International Journal of Time-Critical Computing. 52 (1): 113-122. Springer. January 2016.
19) Luís Miguel Pinho, Vincent Nélis, Patrick Meumeu Yomsi, Eduardo Quiñones, Marko Bertogna, Paolo Burgio, Andrea Marongiu, Claudio Scordino, Paolo Gai, Michele Ramponi, Michal Mardiak, "*P-SOCRATES: A parallel software framework for time-critical many-core systems"*, Microprocessors and Microsystems. 39 (8): 1190-1203. Elsevier. November 2015.
20) Robert Davis, Alan Burns, Jose Marinho, Vincent Nelis, Stefan Petter, Marko Bertogna. "*Global and Partitioned Multiprocessor Fixed Priority Scheduling with Deferred Pre-emption*", ACM Transactions on Embedded Computing Systems. 14 (3): Article 47, May 2015.
21) Giorgio Buttazzo, Marko Bertogna, Gang Yao. *"Limited Preemptive Scheduling for Real-Time Systems: a Survey"*, IEEE Transactions on Industrial Informatics. 9(1): 3-15. February 2013.
22) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Feasibility Analysis under Fixed Priority Scheduling with Limited Preemptions"*, Real-Time Systems: The International Journal of Time-Critical Computing. 47(3): 198-223. Springer. May 2011.
23) Marko Bertogna, Sanjoy Baruah. *"Tests for global EDF schedulability analysis"*, Journal of Systems Architecture. 57(5): 487-497. Elsevier. May 2011.
24) Marko Bertogna, Sanjoy Baruah. *"Limited preemption EDF scheduling of sporadic task systems"*, IEEE Transactions on Industrial Informatics. 6(4): 579-591. November 2010.
25) Marko Bertogna, Nathan Fisher, Sanjoy Baruah. *"Resource-sharing servers for Open Environments"*, IEEE Transactions on Industrial Informatics. 5(3): 202-220. August 2009.IEEE. **Best paper award IEEE Transactions on Industrial Informatics 2010**.
26) Marko Bertogna, Michele Cirinei, Giuseppe Lipari. *"Schedulability analysis of global scheduling algorithms on multiprocessor platforms"*, IEEE Transactions on Parallel and Distributed Systems. 20(4): 553-566. April 2009.
27) Marko Bertogna, Nathan Fisher, Sanjoy Baruah. *"Resource holding times: Computation and Optimization"*, Real-Time Systems: The International Journal of Time-Critical Computing. 41(2): 87-117. Springer. February 2009.
28) Thedor P. Baker, Michele Cirinei, Marko Bertogna. *"EDZL scheduling analysis"*, Real-Time Systems: The International Journal of Time-Critical Computing. 40(3): 264-289. Springer. December 2008.
29) Marko Bertogna, Michele Cirinei, Giuseppe Lipari. *"New schedulability tests for real-time task sets scheduled by Deadline Monotonic on multiprocessors"*, Lecture Notes in Computer Science. 3974/2006: 306-321. Elsevier. 2006.

Peer-Reviewed International Conferences and Workshops

30) Micaela Verucchi, Mirco Theile, Marco Caccamo, Marko Bertogna, "*Latency-aware generation of single-rate DAGs from multi-rate task sets*", IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2021), April 2021.

31) Ignacio Sanudo Olmedo, Nicola Capodieci, Jorge Luis Martinez, Andrea Marongiu, Marko Bertogna, "*Dissecting the CUDA scheduling hierarchy: a Performance and Predictability Perspective*", IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2021), April 2021.
32) Carmelo Scribano, Davide Sapienza, Giorgia Franchini, Micaela Verucchi, Marko Bertogna, "*All You Can Embed: Natural Language based Vehicle Retrieval with Spatio-Temporal Transformers*", Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, 2021.
33) Micaela Verucchi, Luca Bartoli, Fabio Bagni, Francesco Gatti, Paolo Burgio, Marko Bertogna, "*Real-Time clustering and LiDAR-camera fusion on embedded platforms for self-driving cars*", Fourth IEEE International Conference on Robotic Computing (IRC), November 2020.
34) Micaela Verucchi, Gianluca Brilli, Davide Sapienza, Mattia Verasani, Marco Arena, Francesco Gatti, Alessandro Capotondi, Roberto Cavicchioli, Marko Bertogna, Marco Solieri, "*A systematic assessment of embedded neural networks for object detection*" IEEE International Conference on Emerging Technologies and Factory Automation (ETFA), September 2020.
35) Claudio Scordino, Ida Maria Savino, Luca Cuomo, Luca Miccio, Andrea Tagliavini, Marko Bertogna, Marco Solieri, "*Real-Time Virtualization For Industrial Automation*", 25th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA), September 2020.
36) Nicola Capodieci, Roberto Cavicchioli, Ignacio Sañudo Olmedo, Marco Solieri, Marko Bertogna, "*Contending memory in heterogeneous SoCs: Evolution in NVIDIA Tegra embedded platforms*", IEEE 26th International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), August 2020.
37) Gero Schwäricke, Tomasz Kloda, Giovani Gracioli, Marko Bertogna, Marco Caccamo, "*Fixed-priority memory-centric scheduler for COTS-based multiprocessors*", 32nd Euromicro Conference on Real-Time Systems (ECRTS 2020), July 2020.
38) José Martins, Adriano Tavares, Marco Solieri, Marko Bertogna, Sandro Pinto, "*Bao: A lightweight static partitioning hypervisor for modern multi-core embedded systems*", Workshop on Next Generation Real-Time Embedded Systems (NG-RES 2020), 2020.
39) Roberto Cavicchioli, Nicola Capodieci, Marco Solieri, Marko Bertogna, Paolo Valente, Andrea Marongiu, "*Evaluating Controlled Memory Request Injection to Counter PREM Memory Underutilization*", Workshop on Job Scheduling Strategies for Parallel Processing, May 2020.
40) Falk Wurst, Dakshina Dasari, Arne Hamann, Dirk Ziegenbein, Ignacio Sañudo, Nicola Capodieci, Marko Bertogna, Paolo Burgio, "*System Performance Modelling of Heterogeneous HW Platforms: An Automated Driving Case Study*" Euromicro Conference on Digital System Design (DSD 2019), Kallithea, Chalkidiki, Greece, August 2019.
41) Tomasz Kloda, Marco Solieri, Renato Mancuso, Nicola Capodieci, Paolo Valente, Marko Bertogna, "*Deterministic memory hierarchy and virtualization for modern multi-core embedded systems*" 25th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2019), Montreal, Canada, April 2019.
42) Roberto Cavicchioli, Nicola Capodieci, Marco Solieri, Marko Bertogna, "*Novel Methodologies for Predictable CPU-To-GPU Command Offloading*", 31st Euromicro Conference on Real-Time Systems (ECRTS 2019), Stuttgart, Germany, July 2019.
43) Nicola Capodieci, Roberto Cavicchioli, Marko Bertogna, Aingara Paramakuru, "*Deadline-based Scheduling for GPU with Preemption Support*", 39th IEEE Real-Time Systems Symposium (RTSS 2018), Nashville, Tennessee, USA, December 2018.
44) Nicola Capodieci, Roberto Cavicchioli, Marko Bertogna, Aingara Paramakuru, "*NVIDIA GPU Scheduling details in Virtualized environments*", International Conference on Embedded Software (EMSOFT) – Work in Progress paper, Turin, Italy, October 2018.
45) Paolo Burgio, Gianluca Brilli, Antonio Marra, Marko Bertogna, "*Convolutional Neural Networks on embedded automotive platforms: a qualitative comparison*", 6th International Workshop on Advances in Parallel Programming Models and Frameworks for the Multi-/Many-core Era (APPMM 2018), in conjunction with 16th International Conference on High Performance Computing & Simulation (HPCS 2018), Orleans, France, July 2018.
46) Paolo Burgio, Christian Di Biagio, Franco Felici, Giovanni Nuzzo, Marko Bertogna, "*The Key Role of Memory in Next-Generation Embedded Systems for Military Applications*", 6th International Conference in Software Engineering for Defense Applications (SEDA 2018), Rome, Italy, June 2018.
47) Eduardo Quiñones, Marko Bertogna, Erez Hadad, Ana Juan Ferrer, Luca Chiantore, Alfredo Reboa. *"Big Data Analytics for Smart Cities: The H2020 CLASS Project".* Proceedings of the 11th ACM International Systems and Storage Conference (SYSTOR '18), Haifa, Israel, June 2018.

48) Ignacio Sanudo, Paolo Cortimiglia, Paolo Burgio, Christian Di Biagio, Franco Felici, Giovanni Nuzzo, and Marko Bertogna "*The key role of memory in next-generation embedded systems for military application*", Software Engineering for Defence Applications (SEDA 2017), Rome, Italy, June 2018.
49) Paolo Burgio, Gianluca Brilli, Antonio Marra, Marko Bertogna, "*Convolutional Neural Networks on embedded automotive platforms: a qualitative comparison*", Workshop on New Platforms for Future Cars: Current and Emerging Trends, in conjunction with Design, Automation and Test in Europe (DATE 2018), Dresden, Germany, March 2018.
50) Eduardo Quiñones, Marko Bertogna, Erez Hadad, Ana Juan Ferrer, Luca Chiantore, Alfredo Reboa. *"Big Data Analytics for Smart Cities: The H2020 CLASS Project".* Workshop on New Platforms for Future Cars: Current and Emerging Trends, in conjunction with Design, Automation and Test in Europe (DATE 2018), Dresden, Germany, March 2018.
51) Nicola Capodieci, Roberto Cavicchioli, Paolo Valente and Marko Bertogna, "*SiGAMMA: Server based integrated GPU Arbitration Mechanism for Memory Accesses*", Proceedings of the 25th International Conference on Real-Time Networks and Systems (RTNS'17), Grenoble, France, October 2017.
52) Nicola Capodieci, Roberto Cavicchioli and Marko Bertogna, "*Memory Interference Characterization between CPU cores and integrated GPUs in Mixed-CriticalityPlatforms*". Proceedings of 22nd IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2017), Limassol, Cyprus, September 2017.
53) Ignacio Sañudo Olmedo, Paolo Burgio and Marko Bertogna, "*An emulation framework for closed source components in multi-core automotive platforms*", Forum on specification & Design Languages (FDL) 2017 – Special Session on Design and test of Automotive Embedded System, Verona, Italy, September 2017.
54) Marko Bertogna, Paolo Burgio, Giacomo Cabri and Nicola Capodieci, "*Adaptive Coordination in Autonomous Driving: Motivations and Perspectives*", Proceedings of the IEEE 26th International Conference on Enabling Technologies: Infrastructure for Collaborative Enterprises (WETICE'17), Poznan, Poland, August 2017.
55) Ignacio Sañudo, Paolo Burgio and Marko Bertogna, "*HGT: An Open-Source Framework for Simulating Parallel Real-Time Tasks*", Proceedings of 8th International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS), in conjunction with 29th Euromicro Conference on Real-Time Systems (ECRTS '2017), Dubrovnik, Croatia, June 2017.
56) Jorge Martinez, Ignacio Sañudo, Paolo Burgio and Marko Bertogna, "*End-To-End Latency Characterization of Implicit and LET Communication Models*", Proceedings of 8th International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS), in conjunction with 29th Euromicro Conference on Real-Time Systems (ECRTS 2017), Dubrovnik, Croatia, June 2017.
57) Maria A. Serrano, Alessandra Melani, Sebastian Kehr, Marko Bertogna and Eduardo Quiñones, "*An Analysis of Lazy and Eager Limited Preemption Approaches under DAG-Based Global Fixed Priority Scheduling*", Proceedings of the 20th IEEE International Symposium on Real-Time Distributed Computing (ISORC'17), Toronto, Canada, May 2017. ACM SIGBED Review 15 (1), 57-63.
58) Alessandra Melani, Maria A. Serrano, Marko Bertogna, Isabella Cerutti, Eduardo Quinones, Giorgio Buttazzo. *"A static scheduling approach to enable safety-critical OpenMP applications"*, Proceedings of the 22nd Asia and South Pacific Design Automation Conference (ASP-DAC 2017), Chiba/Tokyo, Japan, January 2017.
59) Alessandro Biondi, Giorgio C. Buttazzo, Marko Bertogna. *"Partitioning and Interface Synthesis in Hierarchical Multiprocessor Real-Time Systems"*, Proceedings of the 24th International Conference on Real-Time Networks and Systems (RTNS'16), Brest, France, October 2016. **Outstanding Paper Award.**
60) Ignacio Sañudo, Roberto Cavicchioli, Nicola Capodieci, Paolo Valente, Marko Bertogna. *"A Survey on Shared Disk I/O Management in Virtualized Environments under Real-Time Constraints"*, Proceedings of the Embedded Operating System Workshop (EWiLi'16), in conjunction with the Embedded Systems Week (ESWeek 2016), Pittsburgh PA, USA, October 2016.
61) Paolo Burgio, Marko Bertogna, Ignacio Sanudo Olmedo, Paolo Gai, Andrea Marongiu, Michal Sojka. *"A Software Stack for Next-Generation Automotive Systems on Many-core Heterogeneous Platforms"*, Proceedings of the 9th Euromicro Conference on Digital System Design (DSD 2016), Limassol, Cyprus, August-September 2016.
62) Ignacio Sanudo, Paolo Burgio and Marko Bertogna. *"Schedulability and Timing Analysis of Mixed Preemptive-Cooperative Tasks on a PartitionedMulti-Core System"* , Proceedings of the 7th

International Workshop on Analysis Tools and Methodologies for Embedded and Real-Time Systems (WATERS'16), in conjuction with the 28th Euromicro Conference on Real-Time Systems (ECRTS 2016), Toulouse, France, July 2016.

63) Maria Serrano, Alessandra Melani, Marko Bertogna, Eduardo Quiñones. "*Response-Time Analysis of DAG Tasks under Fixed Priority Scheduling with Limited Preemption*" , Proceedings of the Design Automation and Test in Europe (DATE'16), Dresden, Germany, March 2016.
64) Alessandra Melani, Marko Bertogna, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio Buttazzo. "*Memory-Processor Co-Scheduling in Fixed Priority Systems*" , Proceedings of the 23rd International Conference on Real-Time Networks and Systems (RTNS'15), Lille, France, November 2015.
65) Abhilash Thekkilakattil, Robert I. Davis, Radu Dobrin, Sasikumar Punnekkat, Marko Bertogna. "*Multiprocessor Fixed Priority Scheduling with LimitedPreemptions*" , Proceedings of the 23rd International Conference on Real-Time Networks and Systems (RTNS'15), Lille, France, November 2015.
66) Paolo Burgio, Andrea Marongiu, Paolo Valente and Marko Bertogna. "*A memory-centric approach to enable timing-predictability within embedded many-core accelerators*". The CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST'15), Tehran, Iran, October 2015. **Best Paper Award**.
67) Maria A. Serrano, Alessandra Melani, Roberto Vargas, Andrea Marongiu, Marko Bertogna and Eduardo Quinones. "*Timing Characterization of OpenMP4 Tasking Model*", Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES'15), Amsterdam, The Netherlands, October 2015.
68) Alessandra Melani, Marko Bertogna, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio C. Buttazzo. "*Response-Time Analysis of Conditional DAG Tasks in Multiprocessor Systems*", Proceedings of 27th Euromicro Conference on Real-Time Systems (ECRTS 2015), Lund, Sweden, July 2015.
69) Alessandro Biondi, Giorgio C. Buttazzo, Marko Bertogna. "*Supporting Component-based Development in Partitioned Multiprocessor Real-Time Systems*", Proceedings of 27th Euromicro Conference on Real-Time Systems (ECRTS 2015), Lund, Sweden, July 2015. **Outstanding Paper Award.**
70) Vincent Nelis, Patrick Meumeu Yomsi, Luis Miguel Pinho, Eduardo Quiñones, Marko Bertogna, Andrea Marongiu, Paolo Gai and Claudio Scordino. "*A system model and stack for the parallelization of time-critical applications on many-core architectures*", Proceedings of 3rd High-performance and Real-time Embedded Systems (HiRES'15) workshop, in conjunction with 10th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'15), January 2015, Amsterdam, Netherlands.
71) Cláudio Maia, Marko Bertogna, Luís Nogueira, Luis Miguel Pinho, "*Response-Time Analysis of Synchronous Parallel Tasks in Multiprocessor Systems*", Proceedings of the 22nd International Conference on Real-Time Networks and Systems (RTNS'14), Versailles, France, October 2014.
72) Mario Bambagini, Marko Bertogna, Giorgio Buttazzo. "*On the Effectiveness of Energy-Aware Real-Time Scheduling Algorithms on Single-Core Platforms*", Proceedings of the 19th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2014), Barcelona, Spain, September 2014.
73) Luis Miguel Pinho, Eduardo Quinones, Marko Bertogna, Andrea Marongiu, Jorge Pereira Carlos, Claudio Scordino, Michele Ramponi, "*P-SOCRATES: a Parallel Software Framework for Time-Critical Many-Core Systems*", Proceedings of the 17th Euromicro Conference on Digital Systems Design (DSD 2014), Verona, Italy, August 2014.
74) Bo Peng, Nathan Fisher and Marko Bertogna, *"Explicit Preemption Placement for Real-Time Conditional Code"*, Proceedings of 26th Euromicro Conference on Real-Time Systems (ECRTS 2014), Madrid, Spain, July 2014.
75) Alessandro Biondi, Alessandra Melani, Marko Bertogna, Giorgio Buttazzo, *"Optimal Design for Reservation Servers under Shared Resources"*, Proceedings of 26th Euromicro Conference on Real-Time Systems (ECRTS 2014), Madrid, Spain, July 2014.
76) Vincent Nélis, Patrick Meumeu Yomsi, Luís Miguel Pinho, José Carlos Fonseca, Marko Bertogna, Eduardo Quiñones, Roberto Vargas, Andrea Marongiu, "The Challenge of Time-Predictability in Modern Many-core Architectures", Proceedings of 14th International Workshop on Worst-Case Execution Time Analysis (WCET 2014), Madrid, Spain, July 2014.

77) Alessandro Biondi, Alessandra Melani, Marko Bertogna, *"Hard Constant Bandwidth Server: Comprehensive Formulation and Critical Scenarios"*, Proceedings of 9th IEEE International Symposium on Industrial Embedded Systems (SIES 2014), Pisa, Italy, June 2014. **Best Paper Award**.
78) Luis Miguel Pinho, Eduardo Quinones, Marko Bertogna, Luca Benini, Jorge Pereira Carlos, Claudio Scordino, Michele Ramponi, *"Time Criticality Challenge in the Presence of Parallelised Execution"*, Proceedings of 2nd Workshop on High-performance and Real-time Embedded Systems (HiRES 2014), held in conjunction with the 9th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC 2014), Vienna, Austria, January 2014.
79) Jose Marinho, Vincent Nelis, Stefan M. Petters, Marko Bertogna, Robert I. Davis, *"Limited Pre-emptive Global Fixed Task Priority"*, Proceedings of 34th IEEE Real-Time Systems Symposium (RTSS 2013), Vancouver, Canada, December 2013.
80) Robert I. Davis, Alan Burns, Jose Marinho, Vincent Nelis, Stefan M. Petters, Marko Bertogna, *"Global Fixed Priority Scheduling with Deferred Pre-emption"*, Proceedings of the 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), Taipei (Taiwan), August 2013. **Best Paper Award**.
81) Cláudio Maia, Luís Nogueira, Luis Miguel Pinho, Marko Bertogna. *"Response-Time Analysis of Fork/Join Tasks in Multiprocessor Systems"*, WiP session of 25th Euromicro Conference on Real-Time Systems (ECRTS 2013), Paris, France, July 2013.
82) Mario Bambagini, Giorgio Buttazzo, Marko Bertogna. *"Energy-Aware Scheduling for Tasks with Mixed Energy Requirements"*, Proceedings of 4th International Real-Time Scheduling Open Problems Seminar (RTSOPS 2013), Paris, France, July 2013.
83) Rob Davis, Marko Bertogna. *"Optimal FP Scheduling with Deferred Preemptions"*, Proceedings of 11th Workshop on Models and Algorithms for Planning and Scheduling Problems (MAPSP 2013), Pont à Mousson, France, June 2013.
84) Mario Bambagini, Marko Bertogna, Mauro Marinoni, Giorgio Buttazzo. *"An Energy-Aware Algorithm Exploiting Limited Preemptive Scheduling under Fixed Priorities"*, Proceedings of 8th IEEE International Symposium on Industrial Embedded Systems (SIES 2013), Porto, Portugal, June 2013.
85) Mario Bambagini, Marko Bertogna, Mauro Marinoni, Giorgio Buttazzo. *"On the Impact of Runtime Overhead on Energy-Aware Scheduling"*, Workshop on Power, Energy, and Temperature Aware Real-time Systems (PETARS 2013), Philadelphia, USA, April 2013.
86) Giuseppe Lipari, Laurent George, Enrico Bini, Marko Bertogna. *"On the Average Complexity of the Processor Demand Analysis for Earliest Deadline Scheduling"*, Real-time systems: the past, present, and future, York, UK, March 2013.
87) Rob Davis, Marko Bertogna. *"Optimal Fixed Priority Scheduling with Deferred Pre-emption"*, Proceedings of 33rd IEEE Real-Time Systems Symposium (RTSS 2012), San Juan, Puerto Rico, December 2012.
88) Mario Bambagini, Giorgio Buttazzo, Marko Bertogna. *"Energy Saving Exploiting the Limited Preemption Task Model"*, Proceedings of 3rd International Real-Time Scheduling Open Problems Seminar (RTSOPS 12), Pisa, Italy, July 2012.
89) José Marinho, Stefan M. Petters and Marko Bertogna. *"Extending Fixed Task-Priority Schedulability by Interference Limitation"*, Proceedings of 20th International Conference on Real-Time and Network Systems (RTNS 2012), Pont à Mousson, France, November 2012.
90) Marko Bertogna, Giorgio Buttazzo, Gang Yao. *"Improving Feasibility of Fixed Priority Tasks using Non-Preemptive Regions"*, Proceedings of 32nd IEEE Real-Time Systems Symposium (RTSS 2011), Vienna, Austria, December 2011.
91) Marko Bertogna, Nathan Fisher. *"The Explicit Preemption Placement Problem for Real-Time Conditional Code"*, Proceedings of 2nd International Real-Time Scheduling Open Problems Seminar (RTSOPS 11), Porto, Portugal, July 2011.
92) Marko Bertogna, Orges Xhani, Mauro Marinoni, Francesco Esposito, Giorgio Buttazzo. *"Optimal Selection of Preemption Points to Minimize Preemption Overhead"*, Proceedings of the 23rd Euromicro Conference on Real-Time Systems (ECRTS 11), Porto, Portugal, July 2011.
93) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Comparative evaluation of limited preemptive methods"*, Proceedings of the 15th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2010), Bilbao, Spain, September 2010.
94) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Feasibility Analysis under Fixed Priority Scheduling with Fixed Preemption Points"*, Proceedings of the 16th IEEE International Conference on Embedded

and Real-Time Computing Systems and Applications (RTCSA 2010), Macau, China, August 2010. **Best Paper Award**.

95) Marko Bertogna, Giorgio Buttazzo, Mauro Marinoni, Gang Yao, Francesco Esposito, Marco Caccamo. *"Preemption points placement for sporadic task sets"*, Proceedings of 22nd Euromicro Conference on Real-Time Systems (ECRTS 2010), Bruxelles, Belgium, June 2010.

96) Enrico Bini, Marko Bertogna, Sanjoy K. Baruah. *"The Parallel Supply Function Abstraction for a Virtual Multiprocessor"*, Proceedings of Dagsthul Seminar on Scheduling, Schloss Dagstuhl, Leibniz-Zentrum für Informatik, Germany, May 2010.

97) Tullio Facchinetti, Enrico Bini and Marko Bertogna. *"Reducing the Peak Power through Real-Time Scheduling Techniques in Cyber-Physical Energy Systems"*, International Workshop on Energy Aware Design and Analysis of Cyber Physical Systems (in conjunction with CPSWEEK 2010), Stockholm, Sweden, April 2010.

98) Dario Faggioli, Marko Bertogna, Fabio Checconi. *"Sporadic Server Revisited"*, Proceedings of 25th ACM Symposium On Applied Computing (SAC 2010), Sierre, Switzerland, March 2010.

99) Enrico Bini, Marko Bertogna, Sanjoy Baruah. *"Virtual Multiprocessor Platforms: Specification and Use"*, Proceedings of 30th IEEE Real-Time Systems Symposium (RTSS 2009), Washington, D.C., USA, December 2009.

100) Marko Bertogna. *"Evaluation of existing schedulability tests for global EDF"*, Proceedings of Real-time systems on multicore platforms: Theory and Practice (in conjunction with ICPP 2009), Vienna, Austria, September 2009.

101) Yifan Wu and Marko Bertogna. *"Improving Task Responsiveness with Limited Preemptions"*, Proceedings of 14th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2009), Palma de Mallorca, Spain, September 2009.

102) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Bounding the Maximum Length of Non-Preemptive Regions Under Fixed Priority Scheduling"*, Proceedings of the 15th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2009), Beijing, China, August 2009.

103) Enrico Bini, Giorgio Buttazzo, Marko Bertogna. *"The Multi Supply Function Resource Abstraction for Multiprocessors: the Global EDF case"*, Proceedings of the 15th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2009), Beijing, China, August 2009. **Best Paper Award**.

104) Dario Faggioli, Michael Trimarchi, Fabio Checconi, Marko Bertogna, Antonio Mancina. *"An Implementation of the Earliest Deadline First Algorithm in Linux"*, Proceedings of the 24th Annual ACM Symposium on Applied Computing (SAC 2009), Honolulu, Hawaii, USA. March 2009.

105) Marko Bertogna, Fabio Checconi, Dario Faggioli. *"Non-Preemptive Access to Shared Resources in Hierarchical Real-Time Systems"*, Proceedings of the 1st Workshop on Compositional Theory and Technology for Real-Time Embedded Systems, Barcelona, Spain (Co-located with RTSS 2008). November 2008.

106) Marko Bertogna, Nathan Fisher and Sanjoy Baruah. *"Static-Priority Scheduling and Resource Hold Times"*, Proceedings of the 15th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2007), Long Beach, CA. March 2007.

107) Nathan Fisher, Marko Bertogna and Sanjoy Baruah. *"Resource-Locking Durations in EDF-Scheduled Systems"*, Proceedings of the 13th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2007), Bellevue, WA. April 2007.

108) Marko Bertogna and Michele Cirinei. *"Response-Time Analysis for Globally Scheduled Symmetric Multiprocessor Platforms"*, Proceedings of the 28th IEEE International Real-Time Systems Symposium (RTSS 2007), Tucson, Arizona. December 2007.

109) Nathan Fisher, Marko Bertogna and Sanjoy Baruah. *"The Design of an EDF-scheduled Resource-sharing Open Environment"*, Proceedings of the 28th IEEE International Real-Time Systems Symposium (RTSS 2007), Tucson, Arizona. December 2007.

110) Marko Bertogna, Michele Cirinei, Giuseppe Lipari, *"New schedulability tests for real-time task sets scheduled by Deadline Monotonic on multiprocessors"*, 9th International Conference on Principles of Distributed Systems (OPODIS 2005), Pisa (Italy), December 2005.

111) Marko Bertogna, Michele Cirinei, Giuseppe Lipari, *"Improved schedulability analysis of EDF on multiprocessor platforms"*, 17th Euromicro Conference on Real-Time Systems (ECRTS 2005), Mallorca (Spain), June 2005. **Best Paper Award**.

112) Babaud, Groen, Leijtens, M. Bertogna, J. den Besten, Barbarin, Oei, Karouta, Binsma, and M.K. Smit, *"First integrated continuously tunable AWG-based laser using electro-optical phase shifters"*, 12th European Conference on Integrated Optics (ECIO 2005), Grenoble, April 6-8, 2005.

Proceedings and Editorial

113) M. Bertogna. Proceedings of the *29th Euromicro Conference on Real-Time Systems (ECRTS 2017)*, Dubrovnik, Croatia, July 27-30, 2017.
114) M. Caccamo, M. Bertogna. *Special Issue on Multicore Systems.* Real-Time Systems, 52 (4). 2016.
115) M. Bertogna, L.M. Pinho, E. Quinones. Proceedings of the *21st Ada-Europe International Conference on Reliable Software Technologies* (Ada-Europe 2016), Pisa, Italy, June 13-17, 2016.
116) M. Bertogna, A. Easwaran. Proceedings of the *6th Real-Time Scheduling Open Problems Seminar* (RTSOPS'15), July 7-10, 2015, Lund, Sweden.
117) M. Bertogna. WiP Proceedings of the *26th Euromicro Conference on Real-Time Systems* (ECRTS 2014), Madrid, Spain, July 8-11, 2014.
118) M. Bertogna, S. Gopalakrishnan. Proceedings of the *5th Real-Time Scheduling Open Problems Seminar* (RTSOPS'14), July 8, 2014, Madrid, Spain.
119) M. Bertogna. WiP Proceedings of the *19th IEEE Real-Time and Embedded Technology and Applications Symposium*, Philadelphia, USA, April 9-11, 2013.

Approved EU Projects Deliverables

120) Marko Bertogna. "*Enhanced scheduler with migration support*", deliverable D3.3.2 for the EU-ICT project P-SOCRATES, March 2016.
121) Marko Bertogna. "*Overall Schedulability Analysis*", deliverable D4.3.2 for the EU-ICT project P-SOCRATES, March 2016.
122) Marko Bertogna. "*Independent Schedulability Analysis*", deliverable D4.3.1 for the EU-ICT project P-SOCRATES, March 2015.
123) Marko Bertogna. "*Simple Partitioned Scheduler*", deliverable D3.3.1 for the EU-ICT project P-SOCRATES, March 2015.
124) Marko Bertogna. "*Resource Allocation Requirements*", deliverable D3.1 for the EU-ICT project P-SOCRATES, April 2014.
125) Giorgio Buttazzo, Marko Bertogna, Gang Yao. *"Analysis of Preemptive and Non-Preemptive Scheduling"*, deliverable D3.4 for the EU-ICT project PREDATOR, January 2011.
126) Marko Bertogna. *"Handling Resource Constraints in Open Environments"*, deliverable D4c for the EU-ICT project ACTORS, January 2010.
127) Marko Bertogna. *"Resource reservation scheme evaluation"*, deliverable D4a for the EU-ICT project ACTORS, January 2009.

Book chapters

128) Sören Berger, Dominik Lamp, Manuel Stein, Thomas Voith, Tommaso Cucinotta, Marko Bertogna. *"Execution & Resource Management in QoS-aware Virtualized Infrastructures"*, in "Achieving Real-Time in Distributed Computing: From Grids to Clouds" ed. Dimosthenis Kyriazis, Theodora Varvarigou and Kleopatra G. Konstanteli, 200-217 (2012), IGI Global.

PhD Thesis

129) Marko Bertogna. *"Real-Time Scheduling Analysis for Multiprocessor Platforms"*, Scuola Superiore Sant'Anna, Pisa, May 2008. Awarded with the **2010 "Giovanni Spitali" Award** for the best PhD thesis of the Scuola Superiore Sant'Anna, Pisa, in the years 2008 and 2009.

Technical Reports

130) Nathan Fisher, Marko Bertogna, Sanjoy Baruah. *"The Design of an EDF-scheduled Resource-sharing Open Environment"*, UNC-CS Tech Report, May 2007.

Master Thesis

131) *"InP-Based Integration of Semiconductor Optical Amplifier and Phase Modulators"*, University of Bologna / Technische Universiteit Delft, July 2002.

Modena, January 10th, 2022
Marko Bertogna